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Dopant- and Trap-Limited Gate Modulation in 2D Tin Halide Perovskite Field-Effect Transistors

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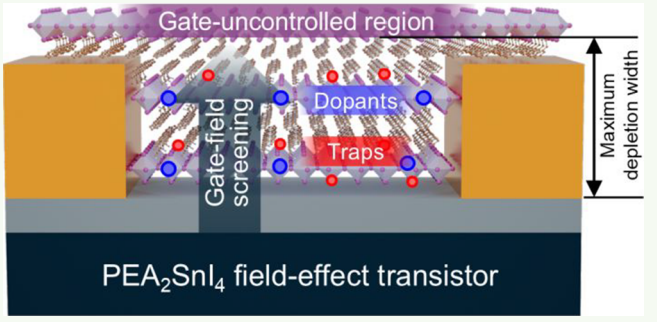
ABSTRACT: Two-dimensional tin halide perovskites have emerged as promising semiconductor materials for next-generation electronics, such as field-effect transistors (FETs), due to their efficient charge transport properties and low-cost, large-area processability. However, the high density of dopants and traps distributed within the bulk channel limits the electrostatic control of halide perovskite FETs. Here, we investigate the impact of channel properties on the device performance of phenethylammonium tin iodide (PEA_2SnI_4) FETs by varying the channel thickness from 34.0 to 305.1 nm. When the channel thickness exceeds a critical value of ~150 nm, corresponding to the maximum depletion width, the devices lose gate modulation, and the on/off ratio collapses to unity. The positive shift in the threshold voltage with thickness indicates a substantial dopant density of $\sim 7.2 \times 10^{16}$ cm^{-3}, and the degradation of the subthreshold swing with thickness suggests a high density of deep bulk traps, calculated to be $\sim 10^{18}$ cm^{-3} eV^{-1}. Furthermore, the analysis of channel crystallinity indicates that a sufficient channel thickness is required for continuous film coverage and that grain boundaries can act as a significant source of apparent bulk traps. Our findings elucidate the effects of dopants and traps within the perovskite channel, suggesting that maximizing gate modulation requires scaling down the channel thickness to the lower limit imposed by the formation of densely packed grains.



KEYWORDS: *field-effect transistors, halide perovskites, gate modulation, dopants, deep traps*

INTRODUCTION

Metal halide perovskites have been widely developed in semiconductor research over the past decades, driving remarkable progress in optoelectronic devices such as photovoltaics, photodetectors, and light-emitting diodes, due to their high optical absorption, long carrier diffusion lengths, and compatibility with low-cost, large-area fabrication.[1−6] Beyond optoelectronics, their high intrinsic carrier mobility has also attracted interest in adopting perovskites for electronic devices, such as channel materials for field-effect transistors (FETs).[7−11] While early research centered on lead (Pb)-based perovskites, their intrinsic toxicity and field-induced ion migration present barriers to further application.[12−14] In response, tin (Sn)-based compositions, such as formamidinium tin iodide ($FASnI_3$) and cesium tin iodide ($CsSnI_3$), have emerged as attractive p-type semiconductors, offering high intrinsic mobility while mitigating the environmental concerns associated with lead.[15,16] In addition, two-dimensional (2D) layered perovskites, including phenethylammonium tin iodide (PEA_2SnI_4), have been developed, where bulky organic cations are inserted between the inorganic perovskite slabs.[17−19] These organic spacer layers effectively suppress ion drift and enhance the environmental stability of 2D perovskites while preserving efficient in-plane charge transport.[20]

However, achieving reliable tin halide perovskite-based electronic devices remains hindered by material limitations.[21−23] Specifically, tin vacancies act as acceptors that unintentionally self-dope the film,[24,25] and point defects and grain boundaries act as deep traps for mobile carriers.[26,27] Moreover, in solution-processed films, processing parameters, such as precursor composition, temperature, or concentration, govern film quality in a complex manner, determining multiple physical properties.[28−31] For instance, changing the precursor concentration affects not only the film thickness but also the crystallinity, including the grain size.[32,33] Therefore, a variety of techniques, such as deep-level transient spectroscopy, space-charge limited

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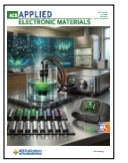

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current analysis, and time-resolved photoluminescence, have been employed to characterize perovskite materials.[34−36] In particular, the FET structure provides a powerful analytical platform for electrical characterization. Beyond its role as a practical switching device, the FET is highly sensitive to carrier concentration and trap states, making it useful for probing the electrical properties of the channel. Moreover, varying the geometrical parameters of FETs enables separating bulk channel contributions from interface effects. Analogous to the transmission line method, where channel length variation isolates transport properties from contact resistance,[37] varying the channel thickness enables separating bulk-dominant behaviors (which scale with the channel thickness) from interface-dominant behaviors (which are independent of the channel thickness).[38]

In this work, we investigate the electrical properties of 2D tin halide perovskite PEA_2SnI_4 FETs with channel thicknesses ranging from 34.0 to 305.1 nm, controlled by precursor concentration. We found that thicker films fabricated from higher precursor concentrations exhibit enhanced conduction driven by enlarged grains, whereas they suffer from a degradation of gate modulation due to the increasing contributions of dopants and traps within the channel. The on/off ratio collapses to unity once the channel thickness exceeds a maximum depletion width of ∼150 nm, providing a thickness limit for gate control. The threshold voltage increases linearly with the channel thickness, yielding a substantial dopant density of $\sim 7.2 \times 10^{16}$ cm^{-3}. Furthermore, the subthreshold swing steadily degrades as the thickness increases, indicating the progressive significance of deep bulk traps in thicker channels, with a high density of $\sim 10^{18}$ cm^{-3} eV^{-1}. The analysis of film crystallinity reveals that sufficient channel thickness is necessary for continuous film coverage and that traps at grain boundaries can serve as a source of apparent bulk traps. Our study highlights the pronounced influence of dopants and traps on device performance, demonstrating that efficient gate modulation requires scaling down the channel thickness to the minimum while ensuring the formation of densely packed grains.

■ RESULTS AND DISCUSSION

Fabrication and Thickness Control of PEA_2SnI_4 Perovskite Transistors

We fabricated two-dimensional perovskite field-effect transistors using PEA_2SnI_4 as a channel material with varying thicknesses (Figure 1a). The devices adopt a bottom-gate/bottom-contact structure on heavily p-doped silicon substrates capped with a 270 nm SiO_2 gate dielectric. The source and drain electrodes were composed of Au (30 nm)/Ti (3 nm). The PEA_2SnI_4 channel was deposited by a single-step spin-coating process in a nitrogen-filled glovebox. The thickness (t_{ch}) of the PEA_2SnI_4 channel in the perovskite FETs (34.0–305.1 nm) was controlled by varying the precursor concentration (0.06–0.36 M) and the spin speed (2500–6000 rpm), followed by thermal annealing (see the Experimental Section for detailed information). Channel thickness mainly scales linearly with the precursor concentration (Figure 1b), whereas spin speed has a minor influence (Figure S1). The fabricated devices were sealed in a N_2-purged metal canister to prevent exposure to oxygen, humidity, and light and then transferred to a probe station for outgassing under high-vacuum conditions ($\sim 10^{-4}$ Torr) for 1 h before the electrical measurements.[39] UV–visible

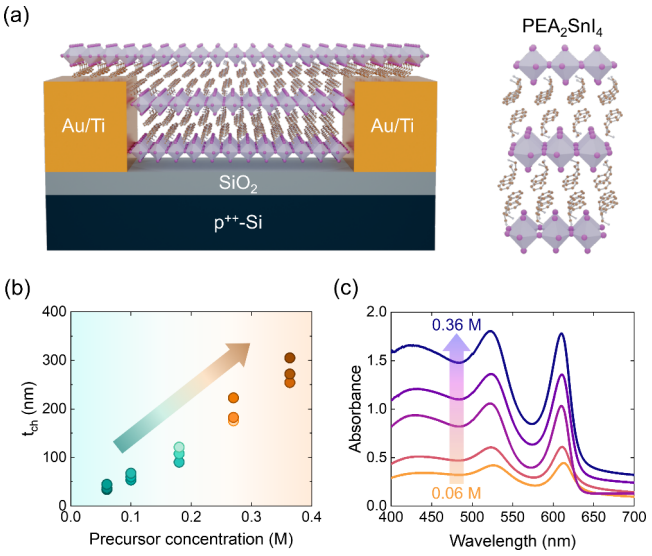

Figure 1. (a) Cross-sectional schematic of a bottom-gate, bottom-contact perovskite FET with the Au/Ti source and drain electrodes, PEA_2SnI_4 channel, SiO_2 gate dielectric, and heavily doped p^{++}-Si gate. (b) Channel thickness (t_{ch} = 34.0–305.1 nm) as a function of precursor concentration shows that the thickness depends linearly on the precursor concentration (0.06–0.36 M). (c) UV–visible absorption spectra of five representative PEA_2SnI_4 films spanning the range of precursor concentrations.

absorption spectra of various films with different concentrations (0.06–0.36 M) exhibit absorption peaks at 432, 523, and 611 nm (Figure 1c), consistent with previous reports on PEA_2SnI_4.[40,41] The Tauc plot analysis yields a consistent optical bandgap of 1.97 ± 0.01 eV for all samples (Figure S2). This invariance in optical properties suggests that changing the precursor concentration effectively controls the channel thickness without altering the electronic structure of the PEA_2SnI_4 films.

Thickness-Dependent Gate Modulation and Carrier Transport in Perovskite FETs

We performed electrical measurements to investigate the impact of channel thickness (t_{ch} = 34.0–305.1 nm) on the carrier transport and gate modulation efficiency. A pulsed-bias scheme (5 ms pulse width and 1 s relaxation time between each step) was applied to minimize the effects of ion migration (see Figure S3 for the detailed measurement method).[42] Figure 2a presents the transfer characteristics (drain current versus gate voltage, I_D–V_{GS}) measured at a fixed drain voltage (V_{DS}) of −1 V. All devices show p-type conduction behavior, but exhibit distinct operational characteristics depending on their thicknesses. Thin-channel devices (teal curves) demonstrate transistor-like behavior with both turn-on and turn-off states, whereas thick-channel devices (brown curves) suffer from a loss of gate modulation, exhibiting high off-currents and resistor-like behavior where the current cannot be effectively modulated by the gate voltage. To investigate the possible parasitic leakage pathways, we also evaluated the gate leakage current (I_G) of the devices (Supporting Information, Section 4). The thin-channel device exhibits $I_D \gg I_G$ at the turn-on state, and the thick-channel device displays $I_D \gg I_G$ across the entire gate voltage sweep, indicating that gate leakage is negligibly small and that the inefficient gate modulation does not primarily

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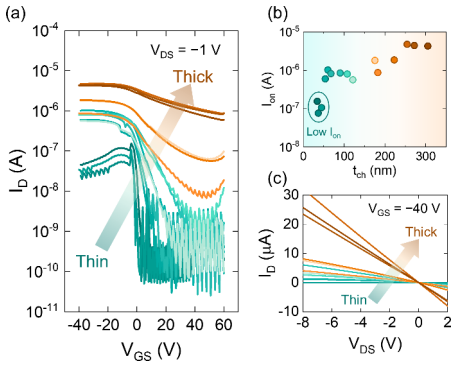

Figure 2. Electrical characteristics of PEA_2SnI_4 FETs with t_{ch} ranging from 34.0 to 305.1 nm. (a) I_D–V_{GS} measured at V_{DS} = −1 V; devices with thin and thick channels are shown as teal and brown curves, respectively. (b) I_{on} as a function of t_{ch}; the three thinnest devices exhibit low I_{on} and are highlighted by a teal-colored circle. (c) I_D–V_{DS} measured at V_{GS} = −40 V.

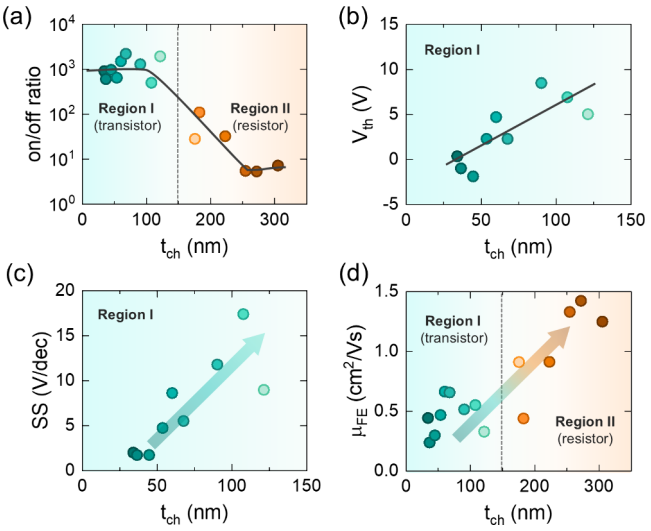

Figure 3. Thickness dependence of key device parameters of PEA_2SnI_4 FETs. (a) On/off ratio of PEA_2SnI_4 FETs versus t_{ch} exhibits two distinct regions. Devices in Region I (thin channels; transistor-like operation) display on/off switching behavior, whereas devices in Region II (thick channels; resistor-like operation) lose gate modulation. The dashed line corresponds to the boundary between the two regions. (b) V_{th} and (c) SS extracted from the devices in Region I. (d) μ_{FE} for all devices.

originate from gate leakage. The on-current (I_{on}; defined as the maximum current) generally increases with t_{ch} (Figure 2b), but a deviation is observed for the three thinnest devices (circled in Figure 2b). We attribute this trend not to the direct effect of channel thickness, but to the crystallinity, specifically incomplete film coverage at low precursor concentrations (further discussion in a later section). The output characteristics (drain current versus drain voltage, I_D–V_{DS}) measured at a fixed V_{GS} = −40 V confirm the enhanced conductance in thicker films (Figure 2c), consistent with the results from the transfer curves. Furthermore, the ohmic-like behavior of the output curves across all thicknesses indicates that the metal–semiconductor contact of the devices does not significantly limit carrier transport properties.[43,44] To quantify this, we extracted width-normalized contact resistance (R_CW) using the transmission line method (TLM) for representative thin and thick devices (t_{ch} = 54.3 and 218.8 nm) (Supporting Information, Section 5). The extracted R_CW values are (2.98 ± 0.40) × 10^4 Ω cm and (5.94 ± 2.69) × 10^3 Ω cm, respectively, which are consistent with the typical range of contact resistance reported for PEA_2SnI_4 FETs using Au contacts.[37,44,45] Since contact resistance becomes significant when I_D is high, the failure of thick-channel devices to turn off is not primarily attributed to contact-related effects. This also supports that the loss of gate modulation originates from unmodulated bulk channels.

We extracted electrical parameters from the transfer curves to quantitatively investigate gate modulation and carrier transport properties (Figure 3; extraction procedures for threshold voltage and field-effect mobility are provided in the Supporting Information, Section 6). The most characteristic trend is the collapse of the on/off ratio to unity, once t_{ch} exceeds a critical thickness of ∼150 nm (Figure 3a). This defines two operational regions: Region I (t_{ch} < ∼150 nm, transistor-like) where the device can be turned off and Region II (t_{ch} > ∼150 nm, resistor-like) where the device cannot be turned off. Within Region I, the devices become progressively difficult to turn off, showing that the threshold voltage (V_{th}) shifts positively with t_{ch} (Figure 3b). This linear dependence yields a bulk dopant density (N_A) of (7.2 ± 2.0) × 10^{16} cm^{-3}, using the relation of $V_{th} = V_{FB} + (qN_A/C_{ox})t_{ch}$, where V_{FB} is the flat-band voltage, q is the elementary charge, and C_{ox} is the gate dielectric capacitance per area. This background hole density is consistent with previous reports on tin halide perovskites,[46−48] highlighting the substantial presence of bulk dopants. A detailed statistical analysis of this extraction method is provided in the Supporting Information, Section 7. In addition to V_{th}, the subthreshold swing (SS) degrades with t_{ch} (Figure 3c). For ideal FETs where deep traps are located solely at the dielectric interface, SS should be independent of channel thickness. In our PEA_2SnI_4 FETs, however, I_D can include contributions from holes across the channel thickness, and trap states within the perovskite channel can also contribute to the thickness-dependent degradation of SS. The SS–t_{ch} trend was further examined by considering possible interface, bulk, and surface trap contributions (Supporting Information, Section 8), supporting that bulk-distributed traps may be involved in the loss of gate modulation in thick channels.

While gate modulation (on/off ratio, V_{th}, and SS) degrades with thickness, charge transport efficiency improves. The field-effect mobility (μ_{FE}) (Figure 3d) shows an upward trend with t_{ch}. This contrasting trend between gate modulation and charge transport arises from their different mechanisms, i.e., the gate modulation is a vertical electrostatic effect limited by the channel thickness, whereas carrier transport is a lateral process governed by in-plane charge scattering (further discussion in a later section). Note that since thick-channel devices (Region II) exhibit inefficient gate modulation, these μ_{FE} values should be interpreted as an apparent field-effect mobility that does not fully reflect gate-controlled carrier transport.

To further examine whether the thickness-dependent gate modulation is preserved beyond the linear operation regime, we also measured transfer characteristics at a higher drain voltage V_{DS} = −40 V, corresponding to saturation mode operation (Supporting Information, Section 9) for the same devices used for the linear mode operation (V_{DS} = −1 V; Figures 2a and 3).

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The electrical properties remain similar to those observed in the linear mode operation: (1) The on/off ratio becomes unity for devices with $t_{ch} > \sim 150$ nm; (2) the threshold voltage positively shifts with increasing channel thickness; (3) the subthreshold swing degrades with channel thickness; and (4) the mobility increases with channel thickness. This consistency between the linear and saturation mode operations supports that the thickness-dependent degradation of gate modulation remains robust with respect to the operation regime and is not a specific artifact of the linear mode analysis.

The devices discussed above were based on the bottom-gate, bottom-contact (BGBC) structure (see Figure 1a). We additionally examined the bottom-gate, top-contact (BGTC) devices with various channel thicknesses (29.2–182.1 nm) (Supporting Information, Section 10). In the BGTC structure, carriers are injected from the top side of the film, whereas the gate field is applied from the bottom dielectric interface. Thus, this structure provides a complementary test of whether the observed thickness dependence is primarily governed by the electrostatic control depth of the bottom gate, rather than by the bottom-contact geometry. The BGTC devices exhibit the same qualitative transition as observed in the BGBC devices: thinner channels retain transistor-like switching, whereas thicker channels show degraded gate modulation. These results suggest that the channel thickness limit for gate modulation is not primarily caused by the bottom-contact configuration but is more closely associated with the finite electrostatic control depth of the bottom gate.

Limit of Gate Modulation in Thick-Channel Transistors by Bulk Dopants and Traps

To understand the degradation of gate modulation (on/off ratio and SS) in thick PEA_2SnI_4 FETs, we investigated the contribution of the bulk channel that scales with channel thickness. First, we address the origin of the critical channel thickness (~150 nm), above which gate modulation is lost, and resistor-like conduction occurs (as shown in Figure 3a). The loss of the off-state can be attributed to the concept of a maximum depletion width ($W_{d,max}$). Figure 4a–c illustrates the energy band diagrams that describe the operational differences between thin- and thick-channel devices. In the on-state ($V_{GS} < V_{FB}$, Figure 4a), a hole accumulation layer forms at the channel/gate dielectric interface regardless of the channel thickness, enhancing current flow. However, to turn the device off ($V_{GS} > V_{FB}$), the gate must entirely deplete free holes distributed throughout the conducting flat-band region. For thin-channel devices where $t_{ch} < W_{d,max}$ (Figure 4b), the depletion width extends throughout the entire channel, effectively insulating the film. Conversely, if $t_{ch} > W_{d,max}$ (Figure 4c), the depletion width saturates at $W_{d,max}$ before reaching the top surface, leaving a parasitic conducting path (from $x = W_{d,max}$ to $x = t_{ch}$) that prevents the device from turning off. We validated this hypothesis of $W_{d,max}$-limited gate control by calculating $W_{d,max}$ as a function of N_A using the one-dimensional Poisson equation for a p-type semiconductor.[49]

$$W_{d,max} = \sqrt{\frac{2\varepsilon_s}{qN_A} 2\phi_F} \tag{1}$$

where ε_s represents the permittivity of the semiconductor channel ($6.3\varepsilon_0$, where ε_0 is the vacuum permittivity),[50] and $2\phi_F$ is the maximum band bending at the dielectric/channel interface. The value of $2\phi_F$ was evaluated to be 1.73 ± 0.03 V using Tauc plot analysis and ultraviolet photoelectron spectroscopy (UPS) measurements (Figures S2 and S13 in the Supporting Information). Substituting the extracted N_A ($(7.2 \pm 2.0) \times 10^{16}$ cm^{-3}, from Figure 3b) into eq 1 yields a theoretical $W_{d,max}$ of 129 ± 18.0 nm, matching the experimentally observed critical thickness of ~150 nm. Note that the estimated uncertainty of $W_{d,max}$ (~14%) is calculated via standard error propagation and is predominantly driven by the standard deviation of N_A (~28%) (Supporting Information, Section 7). This consistency supports that the 'resistor-like' behavior in thick-channel devices arises from an electrostatic limit imposed by the high value of N_A, which is especially significant in tin halide perovskites.[46−48] To ensure proper transistor-like switching behavior, the channel thickness must be geometrically engineered to satisfy $t_{ch} < W_{d,max}$.

In addition to the dopant effect, we investigated the role of trap states in limiting the SS. In conventional silicon FETs, the SS is dominated by interface traps as $D_{it} = \frac{C_{ox}}{q^2}\left(\frac{SS \log_{10} e}{kT/q} - 1\right)$, where D_{it} is the density of states (DOS) of interface traps, and kT is the thermal energy (25.9 meV at 300 K). However, the increase in SS with increasing channel thickness in our devices (Figure 3c) suggests that the contribution of bulk traps (traps distributed throughout the channel volume) becomes progressively more significant relative to that of interface traps. To analyze this trend, we decouple the contributions of bulk traps from interface traps. Figure 4d,e shows the energy profiles of the total carrier density (n_{tot}; containing both trapped and free carriers) and the DOS of bulk traps (D_b) as a function of E_F for four representative devices (t_{ch} = 60.0, 107.6, 175.4, and 254.4 nm). These profiles were calculated from transfer curves and the one-dimensional Poisson equation; thus, we can express the energy profiles of n_{tot} and D_b (extraction details in the Supporting Information, Section 12):

$$n_{tot}(E_F - E_V) = \frac{C_{ox}^2}{q\varepsilon_s}\left(V_{GS} - V_{FB} - \left(1 + \frac{q^2 D_{it}}{C_{ox}}\right)\phi_0\right)\left(1 + \frac{q^2 D_{it}}{C_{ox}} - \left(\frac{d\phi_0}{dV_{GS}}\right)^{-1}\right) \tag{2}$$

and $D_b(E_F - E_V) = dn_{tot}(E_F - E_V)/d(E_F - E_V)$, where ϕ_0 is the band bending at the dielectric/channel interface. To investigate the influence of bulk traps on the efficiency of gate modulation in perovskite FETs, the analysis is separated into the accumulation regime ($E_F - E_V < 0.12$ eV, green region) and the depletion regime ($E_F - E_V > 0.12$ eV, orange region), where $E_F - E_V = 0.12$ eV corresponds to the flat-band condition (Figure S13).

In the accumulation regime, the gate voltage induces positive charges in the channel (see Figure 4a). Figure 4d compares the calculated n_{tot} with the free carrier (hole) density (n_{free}; shown as a black solid line), where n_{free} is calculated using $n_{free} = N_A \exp(-q\phi_0/kT)$. The results show that n_{tot} is comparable to n_{free}, but the difference between them increases as E_F approaches E_V. This difference implies the presence of a sharp distribution of bulk-trap states near the valence band maximum (known as band tail states), which is reflected in the D_b profile in the green region of Figure 4e. By fitting the band tail states

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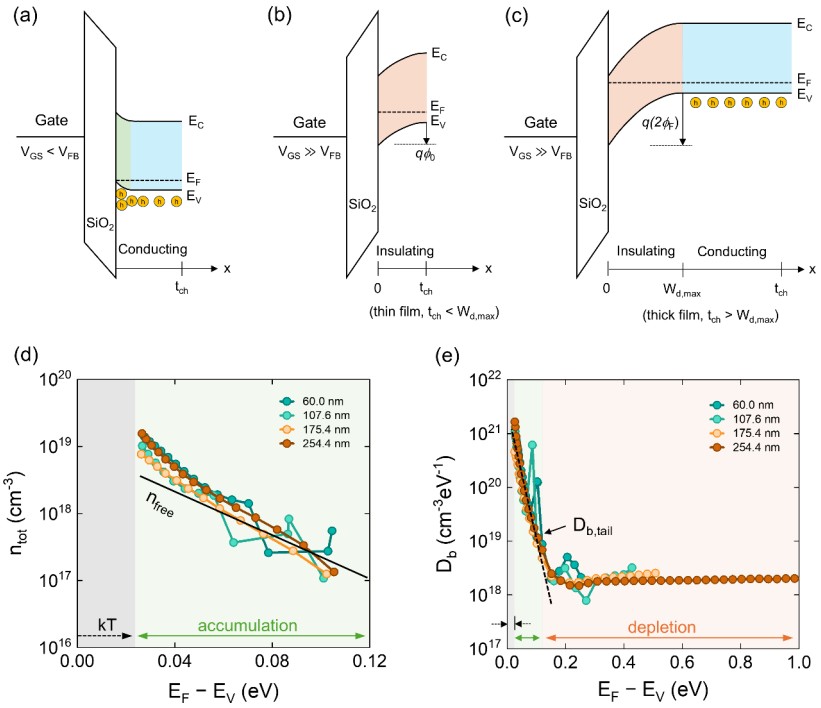

Figure 4. Effect of bulk dopants and traps on gate modulation. (a–c) Energy band diagrams explaining the thickness-dependent on/off behavior. (a) In the accumulation regime ($V_{GS} < V_{FB}$), the Fermi level (E_F) approaches the valence band maximum (E_V), accumulating holes at the dielectric/channel interface (green); conduction occurs via this layer and the pre-existing flat-band bulk holes (blue). (b) Thin-channel device ($t_{ch} < W_{d,max}$): the positive V_{GS} induces interface band bending (ϕ_0), and a large positive V_{GS} ($V_{GS} \gg V_{FB}$) can deplete the entire channel (orange). (c) Thick-channel device ($t_{ch} > W_{d,max}$): ϕ_0 saturates at $2\phi_F$, limiting the depletion width to its maximum value $W_{d,max}$; a residual flat-band region (blue) persists even at high V_{GS}, preventing turn-off. (d) Total carrier density (n_{tot}) vs $E_F - E_V$ in the accumulation regime (green); the black solid line denotes the free carrier density (n_{free}). (e) Bulk-trap DOS (D_b) vs $E_F - E_V$; the black dashed line represents the band tail states ($D_{b,tail}$); green/orange regions mark the accumulation/depletion regimes. Data in (d, e) are from different t_{ch} (60.0, 107.6, 175.4, and 254.4 nm). The gray window ($E_F - E_V < kT = 25.9$ meV (thermal energy at room temperature)) marks where the Boltzmann approximation becomes inaccurate relative to the Fermi–Dirac distribution.

($D_{b,tail}$) to an exponential distribution of energy ($D_{b,tail}(E) \propto \exp(-(E - E_V)/E_U)$, shown as a black dashed line in Figure 4e), we extract an average Urbach energy (E_U) of the devices of 18.2 meV (corresponding to the temperature of 211 K), excluding fitting outliers beyond 1.5σ. Note that this Urbach energy is smaller than thermal energy at room temperature (25.9 meV at 300 K), which implies shallow band tail states near the valence band maximum, consistent with the typical values of E_U reported for halide perovskites from optoelectronic measurements.[51−53]

On the other hand, in the depletion regime ($V_{GS} > V_{FB}$), the interface band bending (ϕ_0) increases, pushing E_F deeper into the bandgap. Therefore, the D_b profile in this region represents deep bulk traps (orange region in Figure 4e), calculated to have an order of magnitude of $\sim 10^{18}$ cm^{-3} eV^{-1} without pronounced features such as peaks in the DOS. This substantial DOS value suggests that the contribution of bulk traps integrated over the film thickness ($D_b t_{ch}$) exceeds the contribution from the interface trap DOS (D_{it}) for thick-channel devices. For instance, with our extracted values (D_{it} $\sim 2.38 \times 10^{12}$ cm^{-2} eV^{-1} and D_b $\sim 10^{18}$ cm^{-3} eV^{-1}; D_{it} is derived from thin devices, see Supporting Information, Section 12), the crossover point where bulk traps become dominant is estimated at $t_{ch} \sim 42$ nm. This significant presence of deep bulk traps explains the trend of SS degradation in thicker films. Moreover, an energy-independent profile of D_b suggests that the deep traps do not originate from a single type of point defect (typically producing a Gaussian-shaped DOS distribution); thus, these results are consistent with contributions from multiple types of defects, including traps located at grain boundaries. Note that our derivation of n_{tot} and D_b approximates the carrier density in the channel using the Boltzmann distribution rather than the Fermi–Dirac distribution. This approximation becomes inaccurate when E_F is very close to E_V ($E_F - E_V < kT$, $kT = 25.9$ meV at 300 K). Therefore, this energy range is excluded from our analysis and is marked as the gray regions in Figure 4d,e (see Section 12 in the Supporting Information for a detailed discussion).

Crystallinity-Dependent Carrier Transport and Trapping

In the previous sections, we observed improved carrier transport in thicker films (I_{on} and μ_{FE}; Figures 2b and 3d) and the significant presence of deep bulk traps (SS and D_b; Figures 3c and 4d). We relate these properties to the polycrystalline nature of the spin-coated perovskite channels, specifically the influence of grain size and the associated grain boundaries. In this section, we investigate the impact of channel crystallinity on the thickness-dependent charge transport. To evaluate the crystallinity of our films, we conducted out-of-plane X-ray diffraction (XRD) measurements (Figure 5a) for films deposited from different precursor concentrations (0.06–0.36 M). The results display sharp (00ℓ) reflections (ℓ = 2, 4, 6, 8, and 10) at nearly the

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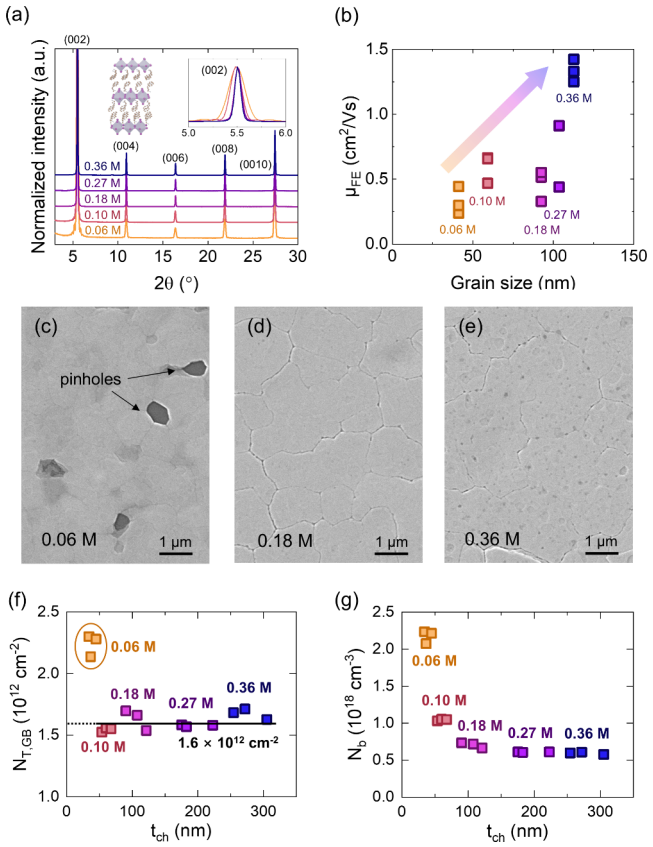

Figure 5. (a) Out-of-plane XRD patterns of films prepared with precursor concentrations of 0.06–0.36 M; the inset shows the enlarged (002) peaks. (b) μ_{FE} as a function of grain size; the grain size is estimated from XRD and color-coded to match panel (a). (c–e) SEM images of films deposited from precursor concentrations of 0.06, 0.18, and 0.36 M. (f) Grain boundary trap density ($N_{T,GB}$) versus t_{ch}; the black solid line represents the average $N_{T,GB}$, excluding the three thinnest devices. (g) Apparent bulk-trap density (N_b) arising from $N_{T,GB}$.

same positions across all films, indicating that the PEA_2SnI_4 crystals are highly oriented with a *c*-axis preference.[54,55] Despite their similar crystal structure, the lateral grain size (calculated from the Scherrer equation)[56,57] exhibits an increase from 41 to 113 nm as the precursor concentration increases. This structural trend provides insights into the apparent thickness-dependent field-effect mobility (Figure 3d). Since the precursor concentration dictates both channel thickness (Figure 1b) and grain size (Figure 5a), the enhanced carrier transport in thicker films is driven by the reduced grain boundary scattering associated with larger grains (Figure 5b), rather than the explicit effect of channel thickness. Top-view scanning electron microscopy (SEM) images (Figure 5c–e) visualize the variation in film coverage governed by the precursor concentration. Films deposited from dilute precursors (0.06 M) exhibit incomplete film coverage (Figure 5c), whereas higher precursor concentrations yield densely packed films (Figure 5d,e). The discontinuity in the film of 0.06 M disrupts the pathways for current flow, explaining the particularly low on-current observed in the thinnest devices (devices circled in Figure 2b). Cross-sectional SEM images further examine the dielectric/channel interface and the bottom-contact edge (Figure S15). These images show that the PEA_2SnI_4 films are continuously formed on the gate dielectric, without gross interfacial voids or film breakage at the perovskite/SiO_2 interface or around the bottom-contact edge within the resolution of SEM. Although these observations do not exclude nanoscale interfacial disorder, they rule out large structural failure at the buried dielectric or contact interfaces as the dominant origin of the thickness-dependent degradation of gate modulation.

In addition to limiting charge transport via scattering, grain boundaries can also introduce trap states that contribute to the degradation of gate modulation. To estimate the possible grain-boundary-related trapping contribution in our devices, we employed the Levinson–Proano method to extract the grain boundary trap density ($N_{T,GB}$, as shown in Figure 5f; the detailed procedure is provided in Figure S17).[58−60] This analysis reveals that $N_{T,GB}$ saturates at $\sim 1.6 \times 10^{12}$ cm^{-2} for fully covered films. Based on the polycrystalline nature of the perovskite channel observed from top-view SEM images (Figure 5c–e) and atomic force microscopy images (Figure S16), we used a simplified square-columnar-grain model to convert $N_{T,GB}$ into an apparent volume trap density (N_b). This conversion is intended as an order-of-magnitude estimate of whether grain boundary-related traps could contribute to an apparent bulk-trap response that scales with channel thickness. Under this assumption, N_b is approximated as $\sim 4 \times N_{T,GB}/(\text{grain size})$ (Figure 5g) (see Supporting Information, Section 15). This estimation yields N_b ranging from $\sim 6 \times 10^{17}$ to $\sim 2.2 \times 10^{18}$ cm^{-3}, implying a substantial density of deep traps (0.7–2.7 traps per 1000 unit cells of PEA_2SnI_4), which is consistent with the high DOS of bulk traps (D_b) calculated in the previous section (Figure 4e). This agreement supports grain boundary-related traps as a plausible contributor to the apparent bulk traps.

Thickness Scaling Limits in Polycrystalline Perovskite FETs

Based on electrical and structural analyses, we investigate the thickness scaling limits for solution-processed 2D perovskite FETs, where the channel thickness and film crystallinity are governed by the precursor concentration. Figure 6a maps the experimental device performance into quadrants defined by the on/off ratio and the on-current (I_{on}), illustrating the trade-off between carrier conduction and electrostatic gate control (Regions I to IV). Devices formed from dilute precursors (Region II) exhibit poor carrier transport due to discontinuous film coverage and small grains, despite the advantage of thin channels for gate modulation. Conversely, devices formed from concentrated precursors (Region IV) exhibit excellent conduction due to enlarged grains, but suffer from a collapse in gate modulation because the channel thickness exceeds the maximum depletion width. The intermediate precursor concentrations (Region I) enable the formation of a continuous film for efficient carrier transport, while maintaining a sufficiently thin channel to minimize the degradation of gate modulation.

Figure 6b schematically summarizes the constraints governing the device operation. While increasing the precursor concentration leads to larger grains and enhances carrier transport (purple trend), channel thickening degrades gate modulation. The increased thickness of the channel results in a higher contribution of bulk dopants (N_A) and traps (D_b) that screen the gate field, degrading the threshold voltage and subthreshold swing. The gate loses electrostatic control once the channel thickness surpasses the limit of the maximum depletion width ($W_{d,max}$, determined by N_A) (dark blue trend). These results

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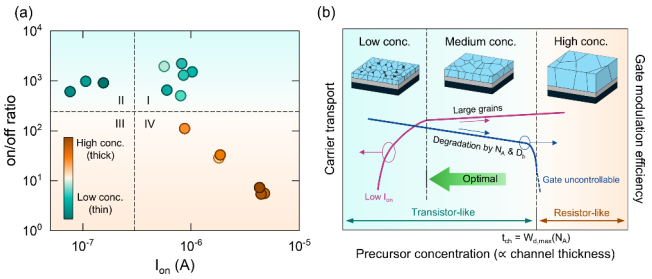

Figure 6. (a) Plot of on/off ratio versus I_{on}, where data points are color-coded by t_{ch} (teal/brown symbols represent thin/thick channels). Devices in Region I (moderate t_{ch}) achieve high I_{on} and high on/off ratios. Region II (low concentration, thin channel) exhibits reduced I_{on} and Region IV (high concentration, thick channel) shows suppressed on/off ratios. (b) Schematic illustration of performance optimization guidelines as a function of the precursor concentration. Low concentrations result in pinhole-rich films with low I_{on}. Increasing the concentration yields densely packed grains, enhancing carrier transport (purple trend), but the resulting increase in channel thickness increases the effects of bulk dopants (N_A) and bulk traps (D_b), thereby suppressing gate modulation. Once t_{ch} exceeds the maximum depletion width $W_{d,max}$, the device cannot be fully turned off (dark blue trend). Thus, the optimal precursor concentration corresponds to the minimum required to achieve densely packed films, thereby forming the thinnest channel without degrading grain connectivity.

suggest a thickness scaling limit for high-performance polycrystalline perovskite FETs, requiring that the channel thickness be minimized while ensuring the formation of densely packed grains.

■ CONCLUSIONS

In summary, we investigated the electrical properties of PEA_2SnI_4 perovskite FETs by varying the channel thickness (34.0–305.1 nm). We estimated a critical thickness of ∼150 nm, corresponding to the maximum depletion width determined by the bulk dopant density (∼7.2 × 10^{16} cm^{-3}). Beyond this thickness, the gate field fails to deplete the entire bulk channel, resulting in the collapse of the on/off ratio to unity. Furthermore, our analysis of bulk traps attributes the degradation of the subthreshold swing to a high density of deep bulk traps (∼10^{18} cm^{-3} eV^{-1}). Structural analysis reveals that a sufficient channel thickness is required to ensure film coverage and that grain boundaries can act as a source of apparent bulk traps. We propose a design guideline for maximizing gate modulation in polycrystalline perovskite FETs, requiring that the channel thickness be minimized while ensuring the formation of densely packed grains. This study provides physical insights into the effects of dopants and traps within the perovskite channel, offering a strategy for maximizing electrostatic modulation in perovskite electronic devices.

■ EXPERIMENTAL SECTION

Precursor Preparation

Precursor solutions of phenethylammonium tin iodide (PEA_2SnI_4), with concentrations ranging from 0.06 to 0.36 M, were prepared by dissolving phenethylammonium iodide (PEAI, 400 mg/mL) and tin iodide (SnI_2, 300 mg/mL) in N,N-dimethylformamide (DMF) at a 2.4:1 molar ratio, including a 20% excess of PEAI for better crystallization.[61] All reagents were purchased from Sigma-Aldrich. The precursor solutions were stirred for 3.5 h at 60 °C in a nitrogen-filled glovebox before film deposition.

Device Fabrication

Highly p-doped Si substrates with thermally grown 270 nm SiO_2 were sequentially cleaned in acetone, isopropanol, and deionized water for 10 min each, followed by drying under a nitrogen flow. Bottom-contact electrodes consisting of Ti (3 nm) and Au (30 nm) were deposited by electron-beam evaporation, patterned through a shadow mask (channel width and length are 1000 and 150 μm, respectively). The substrates were subsequently cleaned again with acetone, isopropanol, and deionized water and exposed to UV-ozone treatment. PEA_2SnI_4 thin films were then deposited by spin-coating the precursor solutions at 2500, 4000, or 6000 rpm, followed by annealing at 100 °C for 10 min inside a nitrogen-filled glove box.

Characterization

The channel thickness of PEA_2SnI_4 films was measured using a surface profiler (ET-200, Kosaka). Film surface morphology was characterized by a field-emission scanning electron microscope (GeminiSEM 560, ZEISS). Out-of-plane X-ray diffraction (D8-Advance, Bruker) was employed to examine crystallinity. UV–visible absorption spectra were acquired using a V-770 spectrophotometer (JASCO). The Fermi level and valence band maximum were determined by ultraviolet photoelectron spectroscopy (Axis Supra+, Kratos). Electrical characteristics of the PEA_2SnI_4 transistors were measured in a vacuum probe station (TTPX, Lake Shore Cryotronics) using a semiconductor parameter analyzer (4200-SCS, Keithley) at room temperature. Detailed transistor analysis procedures are provided in the Supporting Information, Section 6.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsaelm.6c01128.

Channel thickness control of PEA_2SnI_4 perovskite transistors, Tauc plot analysis, pulse-mode biasing scheme for electrical measurements, gate leakage current measurements, transmission line method, FET parameter extraction procedure, statistical evaluation of bulk dopant density, analysis of the subthreshold swing–channel thickness relationship, saturation mode electrical characteristics, electrical properties of bottom-gate/top-contact FETs, ultraviolet photoelectron spectroscopy (UPS) for perovskite films, detailed procedure for bulk-trap analysis, cross-sectional scanning electron microscopy, top-view atomic force microscopy, and Levinson–Proano analysis (DOCX)

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Author Contributions

Jaeyong Woo, **Keehoon Kang**, and **Takhee Lee** designed the experiments; **Jaeyong Woo** fabricated the devices and conducted the electrical measurements; **Jaeyong Woo** and **Seongmin Ko** constructed equations and interpreted the device data; **Youngmin Song**, **Yeeun Kim**, **Sunggyu Ryoo**, and **Taehyun Kong** analyzed optical measurements and assisted in finding overall mechanisms; and **Jaeyong Woo**, **Keehoon Kang**, and **Takhee Lee** wrote the manuscript with all of the authors. All authors contributed to the discussion and preparation of the final manuscript.

Notes

The authors declare no competing financial interest.

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