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ARTICLE

A Vertical Molecular Synaptic Transistor with Redox-Induced Analog States

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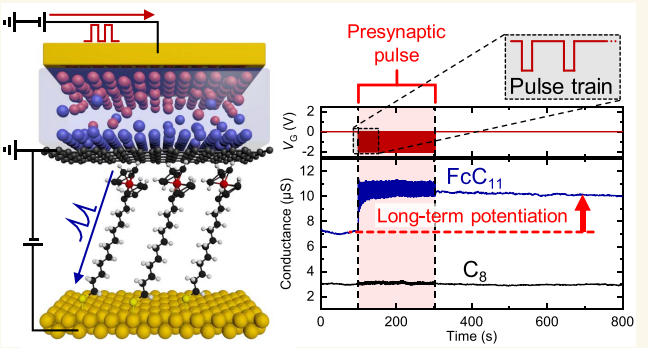
ABSTRACT: We report a three-terminal, ion-gel-gated, redox-active molecular transistor that exhibits synaptic plasticity and analog conductance states. The device was composed of a ferrocene-terminated alkanethiolate self-assembled monolayer as the active channel, vertically sandwiched between a monolayer graphene source and a Au drain, and the channel conductance was modulated by an ion-gel gate. Gate voltage pulses induce an electric double layer at the ion-gel/graphene interface, triggering dynamic postsynaptic-like current responses. Our device exhibited neuroinspired plasticity, including short-term plasticity like paired-pulse facilitation and a programmable transition to long-term plasticity upon repeated stimulation. The ferrocene redox moiety was identified as the key enabler of nonvolatile switching behavior, mediating a dynamic, voltage-programmable conductance change via a synergistic mechanism of reversible redox and ion trapping. In contrast, alkanethiolate control devices without a ferrocene moiety exhibited only volatile, transient responses. We achieved multilevel conductance states with synaptic update characteristics depending on gate pulses, a crucial attribute for the learning process. As a proof of concept, a neural network simulated with our molecular synaptic transistor achieved ∼88% accuracy in MNIST pattern recognition, even after a single training epoch. These results establish vertical molecular transistor systems as promising building blocks for molecular-level neuromorphic hardware, with a three-terminal, read/write-decoupled architecture that exhibits synaptic behavior and helps overcome read-disturb of two-terminal memristive schemes.



KEYWORDS: *molecular electronics, molecular transistors, synaptic devices, ferrocene molecules, neuromorphic computing*

INTRODUCTION

Molecular electronics has advanced tremendously since the first theoretical proposal of a single-molecule rectifier in 1974.[1] Over the past decades, researchers have demonstrated molecular-scale electronic components, including molecular diodes,[2] chemical sensors and energy conversion devices,[3−5] memory,[6] and transistors.[7,8] Of these, the molecular transistors provide a unique platform to exploit the intrinsic properties of molecules by controllably tuning their frontier orbital alignment and coupling with electrodes via an external gate voltage.[9−11]

Meanwhile, the rapid progress of artificial neural networks (ANNs) has spurred demand for hardware implementations of neuromorphic computing, which processes information in a brain-inspired, parallel architecture.[12] A key requirement for neuromorphic hardware is an electronic analog of the synapse—a device whose conductance (synaptic weight) can be gradually modified by electrical stimuli to encode short-term and long-term memory.[13−17] Toward this goal, considerable research has been conducted using a variety of material systems, such as transition-metal oxides, two-dimensional semiconductors, and organic polymers.[18−25] These efforts have produced artificial synapses capable of short-term plasticity (volatile conductance change) and long-term potentiation/depression (nonvolatile conductance change) analogous to biological synapses.[26,27] Notably, even molecular-scale memristors have recently been reported exhibiting synaptic behavior based on the proton-coupled electron transfer in redox molecules[28−30] or electric-field-driven Ag^+ ion migration in a molecular monolayer.[31]

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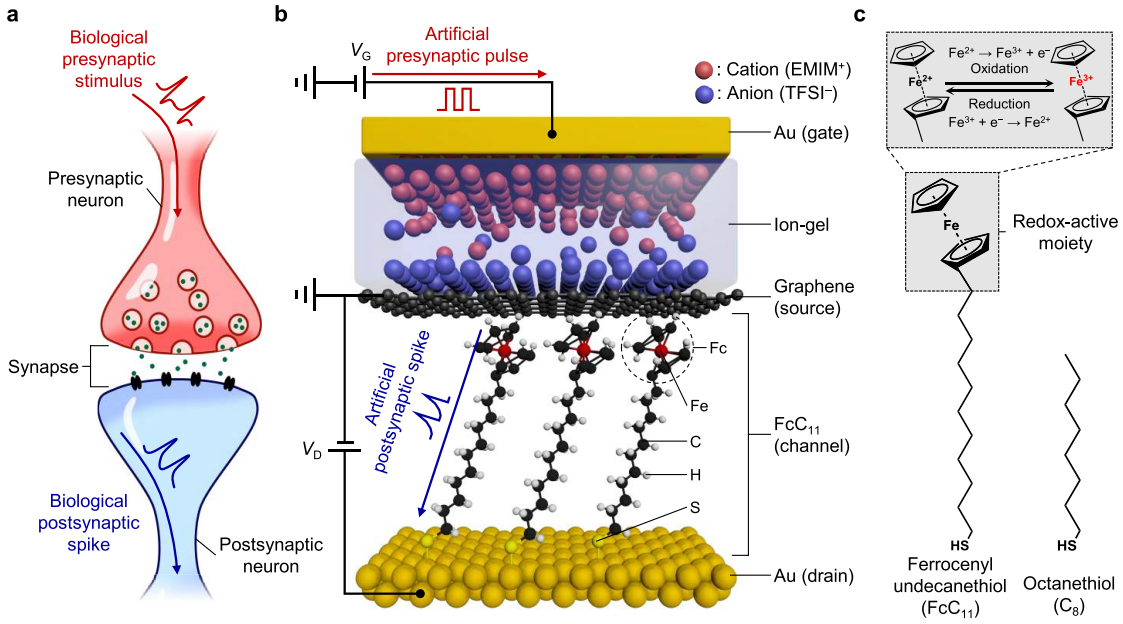

Figure 1. (a) Schematic illustration of a biological synapse showing a presynaptic neuron (red) and a postsynaptic neuron (blue). Applying a presynaptic stimulus induces a postsynaptic spike through the synapse. (b) Structure of an artificial synapse based on a molecular transistor with the channel molecule FcC_{11}. Artificial presynaptic pulses applied to an ion-gel gate induce a change in drain current, which is analogous to a postsynaptic spike. (c) Chemical structures of FcC_{11} and C_8 with illustration of reversible redox chemistry of the Fc moiety.

However, molecular synaptic junctions reported to date have employed two-terminal geometries, in which the read voltage may perturb the stored states because both programming and readout voltage share the same terminal.[32−35] This memristor structure inherently ties the readout bias to the channel's conductance state, potentially causing read-disturb and cumulative read stress that degrades the device's endurance. The three-terminal molecular transistor directly overcomes these challenges. The inclusion of a gate electrode allows for precise control over the conductance of the molecular junction via field effects or ionic dynamics, thereby fundamentally decoupling the "write" and the "read" current paths,[14,16,36] enabling a far more versatile range of learning strategies. This architectural separation makes the gate a dedicated "write" knob for the synaptic weight, while the source−drain path is used only to "read" it, avoiding read-disturb and improving potentiation−depression symmetry in weight updates.

Here, we report a vertical three-terminal molecular synaptic transistor that uses a redox-active ferrocene-alkanethiolate self-assembled monolayer (SAM) as the channel. The device structure combines a monolayer graphene as the top electrode with an ion-gel gate dielectric, enabling electrostatic control of molecular conductance via an electric double layer formed at the graphene interface.[37−39] Applying gate voltage pulses to the ion-gel results in conductance modulation that realizes short-term plasticity (e.g., paired-pulse facilitation) as well as long-term plasticity, including long-term potentiation and long-term depression. In this platform, electrostatic gating governs the conductance of synaptic devices, while the interaction between the redox-active ferrocene (Fc) moiety and anions in the ion-gel is attributed to the volatility or plasticity of the synaptic state. To benchmark the three-terminal molecular synaptic devices, we conducted MNIST and Fashion MNIST simulations based on the measured device characteristics and achieved 88.3 and 75.6% classification accuracy, respectively.

RESULTS AND DISCUSSION

Structure of Synaptic Molecular Transistor Device.

Figure 1a shows the configuration schematic of a biological synapse. Action potentials in the presynaptic neuron trigger the release of Ca^{2+}-dependent neurotransmitters, which bind to receptors on the postsynaptic membrane and generate excitatory or inhibitory postsynaptic currents/potentials.[26,27] The connection strength (synaptic weight) between presynaptic input and postsynaptic response changes with neural activity, showing plasticity over different time scales: short-term (milliseconds to seconds) and long-term (hours to days). Repeated, correlated activities tend to strengthen the synapse, whereas uncorrelated or diminished activities can weaken it, altering the probability and amplitude of postsynaptic spiking.[26,27]

Figure 1b illustrates the ion-gel-gated vertical molecular transistor that emulates essential synaptic behavior. The device structure is a vertical three-terminal junction in which ferrocene undecanethiolate (FcC_{11}) SAM serves as the channel between the monolayer graphene (source) and Au (drain) electrodes. An ion-gel gate dielectric, composed of ionic liquid 1-ethyl-3-methylimidazolium (EMIM) cations and bis-(trifluoromethylsulfonyl)imide (TFSI) anions ([EMIM]-[TFSI]) and a triblock copolymer poly(styrene-*block*-methyl methacrylate-*block*-styrene) (PS-PMMA-PS), covers the graphene electrode and is contacted by a Au gate pad. The thickness of the ion-gel was measured as 5 μm, which is similar to the previously reported value (Figure S7).[40] This configuration enables electrostatic gating through the atomically thin graphene to the underlying SAM, as reported in previous works.[11,38,39] It is notable that the gate field penetrates the graphene even when it is grounded, the mechanism of which is provided in the Supporting Information (Section 6). Detailed explanation of the device fabrication is provided in the Experimental Section and Supporting Information (Section 3). Gate voltage (V_G) pulses serve as

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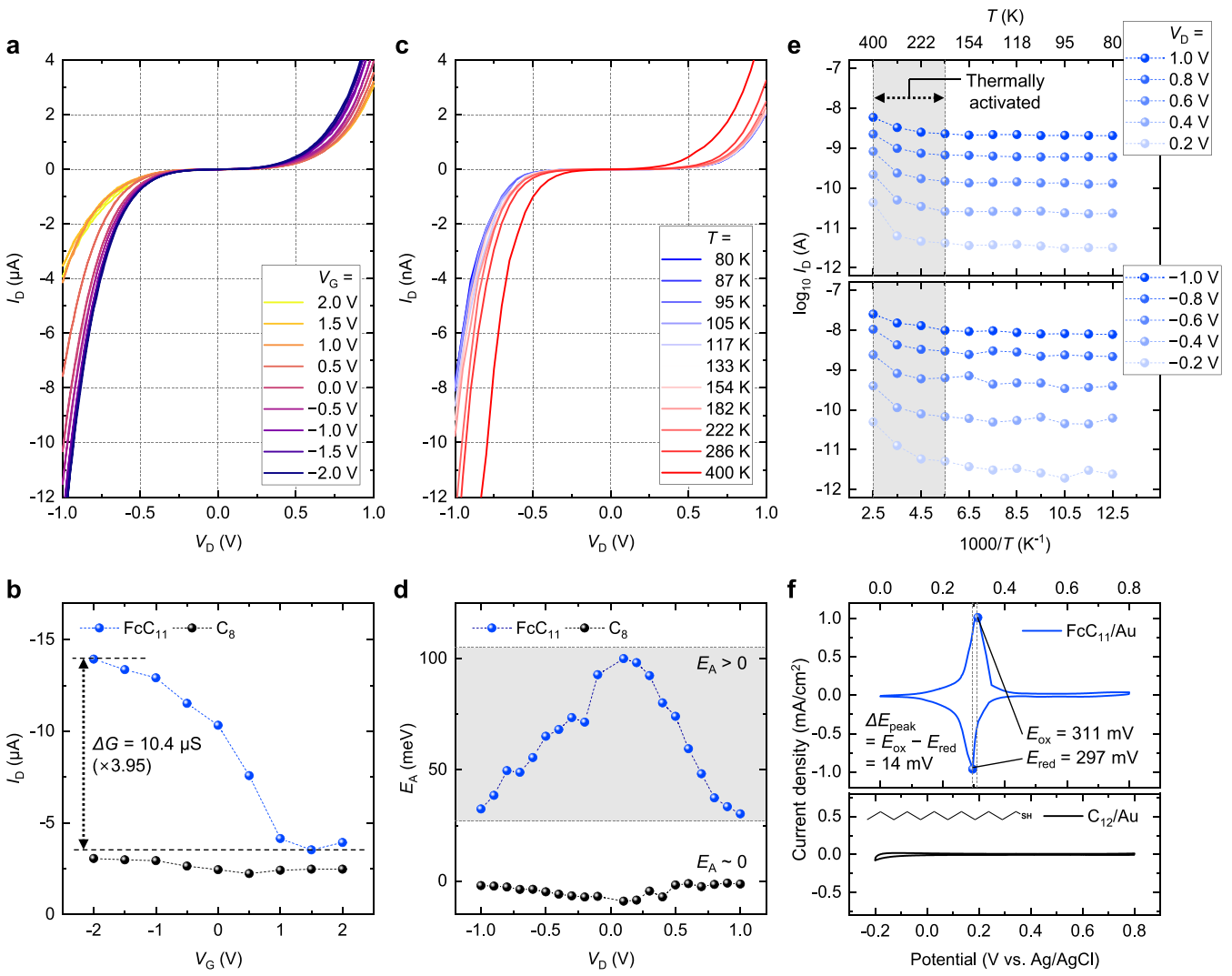

Figure 2. Transport characteristics of FcC_{11} molecular transistors. (a) Output characteristics of the FcC_{11} transistor under static gate voltage ranging from −2.0 to 2.0 V. (b) Transfer characteristics of the FcC_{11} transistor (blue) compared to the C_8 transistor (black) as a control experiment. A 3.95-fold change in channel conductance was observed for the FcC_{11} transistor. (c) Temperature dependence of the drain current of the 2-terminal FcC_{11} junction with a temperature range from 80 to 400 K. (d) Activation energy of the FcC_{11} junction (blue) as a function of drain voltage in comparison with that of the C_8 junction (black) lying near 0 eV. (e) Arrhenius plot of the drain current of the FcC_{11} junction at each drain voltage, showing thermally activated behavior for temperatures above ~180 K. (f) Cyclic voltammetry results of the redox-active FcC_{11}/Au substrate (blue) and redox-inactive C_{12}/Au (black), showing reversible redox properties of the ferrocene moiety in the SAM configuration. The chemical structure of C_{12} is shown as an inset in the lower panel.

artificial presynaptic stimuli, while the resulting changes in drain current (I_D) at a fixed source−drain bias (V_D) are measured as the postsynaptic response. The three-terminal geometry thus allows the independent application of presynaptic-like gate pulses without perturbing the constant V_D used to monitor the postsynaptic signal.

Figure 1c shows the chemical structures of FcC_{11} and octanethiol (C_8). FcC_{11} has a redox-active Fc moiety highlighted as a gray box, which can undergo oxidation (Fc → Fc^+) or reduction (Fc^+ → Fc) with two possible oxidation states of +2 and +3 of the central iron ion. While the redox activity and the synaptic behavior of FcC_{11} transistors are focused here, C_8, a plain alkanethiol without an Fc moiety, is investigated as a control device to probe the effect of redox in the synaptic behavior of molecular transistors. The C_8 control device has the same structure as the FcC_{11} transistor depicted in Figure 1b, except that the FcC_{11} SAM is replaced by the C_8 SAM.

Electrical Characteristics of the FcC_{11} Molecular Transistor and the Redox Signature of FcC_{11} SAM. We characterized the electrical properties of FcC_{11} molecular transistors. Detailed circuit diagrams and their correspondence to the real images of devices are provided in Supporting Information (Section 3). Figure 2a shows the output characteristics (I_D−V_D) of an FcC_{11} device measured at 300 K, showing gate controllability. After applying V_G, we waited 60 s for the electric double layer to reach equilibrium. Then, we conducted consecutive forward and backward V_D sweeps. Specifically, applying negative V_G increases the drain current, whereas positive V_G suppresses it. This indicates highest occupied molecular orbital (HOMO)-mediated conduction (p-type like conduction), which is consistent to previously reported ferrocene-terminated molecular junctions.[41,42] A current asymmetry (i.e., higher current at negative V_D) is observed, which is also consistent with prior reports.[37,42] Also, the devices showed no hysteresis on V_D sweep, which ensures

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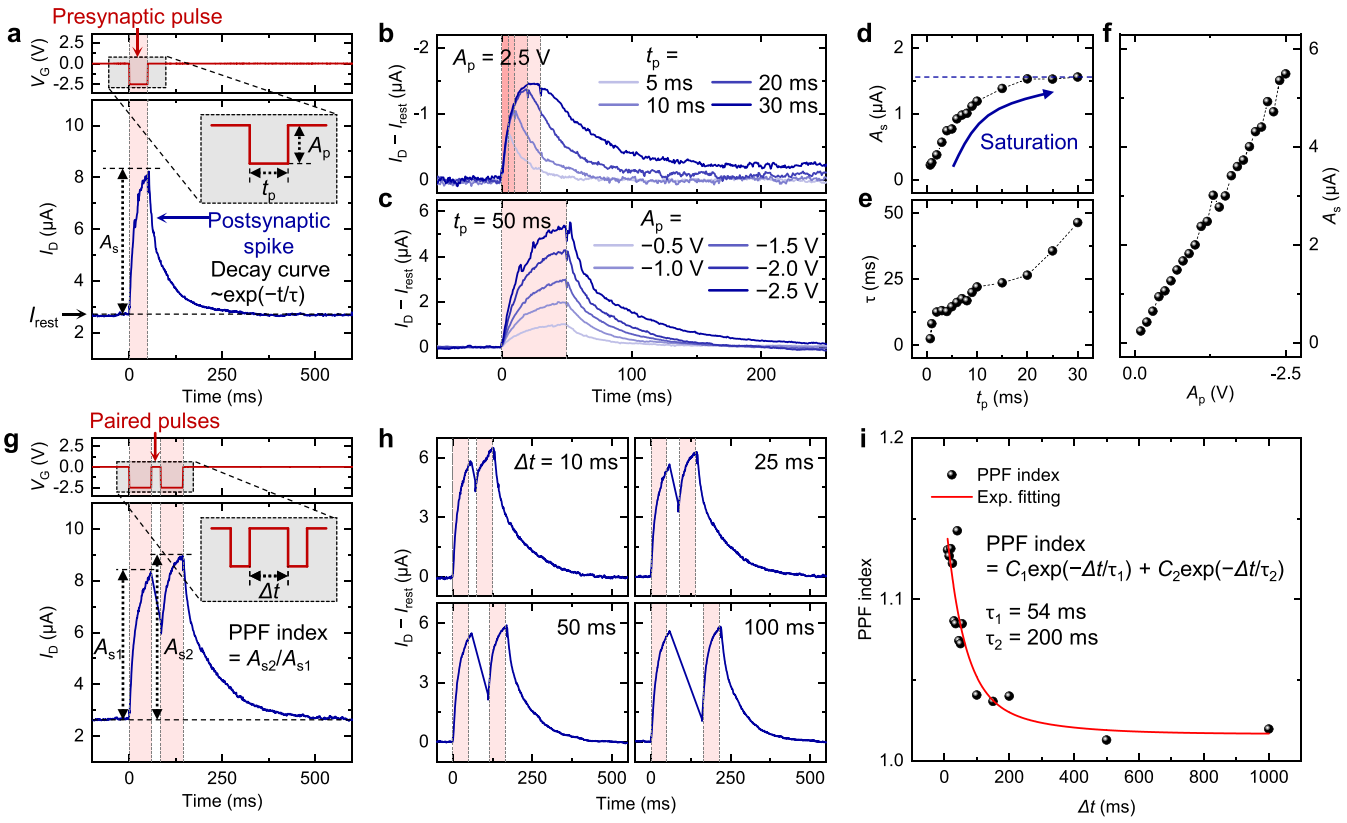

Figure 3. STP and PPF characteristics. (a) Illustration of STP with a presynaptic pulse applied to the gate electrode (top panel) and the corresponding postsynaptic spike measured as the drain current (bottom panel), with definitions of pulse amplitude (A_p) and width (t_p), and the amplitude of the postsynaptic spike (A_s). (b) Representative STP characteristics for varying t_p ranging from 5 to 30 ms, with fixed A_p = 2.5 V. (c) Representative STP characteristics for varying A_p ranging from −0.5 to −2.5 V, with fixed t_p = 50 ms. (d) Change of A_s as a function of t_p, showing saturating behavior at $t_p \sim 30$ ms. (e) Change of τ as a function of t_p, showing s positive correlation. (f) Linear relation between A_p and resulting A_s. (g) Illustration of PPF with a pair of presynaptic pulses applied to the gate electrode (top panel) and the corresponding postsynaptic spike measured as the drain current (bottom panel), with definitions of the interval between pulses (Δt), amplitude of presynaptic spikes for the first and second pulses (A_{s1} and A_{s2}), and the PPF index. (h) Representative PPF characteristics for varying Δt ranging from 10 to 100 ms, with fixed A_p = −2.5 V and t_p = 50 ms. (i) PPF index as a function of Δt (black symbols) and its fitting with a two-phase exponential decay model with two time constants τ_1 and τ_2 (red curve).

the suppressed read-out disturb when implemented as a synaptic device (Figures S21 and S22, Supporting Information). Figure 2b compares transfer curves (I_D−V_G) measured at V_D = −1.0 V for an FcC_{11} molecular transistor and a control device in which C_8 is used instead of FcC_{11} in the channel. The FcC_{11} device exhibits distinct gate tunability with a conductance change of $\Delta G \approx 10.4\ \mu S$ and a ratio G_{max}/G_{min} = 3.95 over the gate sweep, while the C_8 control device shows a very weak response to V_G. This confirms that the pronounced gate dependence arises from the Fc moiety.

To elucidate the charge transport mechanism through the molecular channel, we characterized FcC_{11} junctions in a two-terminal configuration without the ion-gel gate. The I_D−V_D curves measured from 80 to 400 K (Figure 2c) reveal a strong temperature dependence within the V_D range from −1.0 to 1.0 V. Again, the junctions did not show hysteresis in the V_D sweep process (Figures S18 and S19, Supporting Information). The activation energy (E_A) of the current obtained by the relation $I_D \sim e^{-(E_A/k_BT)}$, where k_B is the Boltzmann constant and T is the temperature, is plotted as a function of drain voltage in Figure 2d. While the C_8 control junction remains nearly temperature-independent ($E_A \sim 0$ eV), the FcC_{11} junction showed E_A in the range between 30 and 100 meV (Figure 2d and Figure S15 in the Supporting Information). Arrhenius analysis of the FcC_{11} data (Figure 2e) reveals thermal activation in the temperature range from ∼180 to 400 K (see the gray area in Figures 2d,e), comparable to reported values for ferrocene-based junctions.[41,42] Below ∼180 K, the current shows nearly temperature-independent behavior, where the thermal energy becomes insufficient to overcome the activation barrier. The absence of a measurable E_A in the C_8 control junction supports that the temperature dependence in the FcC_{11} junction is attributed to the redox chemistry of the ferrocene moiety rather than to the measurement system or junction defects. More detailed descriptions of the characterization of FcC_{11} molecular transistors can be found in the Supporting Information (Sections 4 and 5)

Furthermore, cyclic voltammetry on FcC_{11}/Au (Figure 2f) displays a reversible redox activity of the FcC_{11} SAM, with narrow peak separation ($\Delta E_{peak} = E_{ox} - E_{red}$ = 14 mV; cathodic peak potential E_{ox} = 311 mV and anodic peak potential E_{red} = 297 mV versus Ag/AgCl), whereas a control experiment with dodecanethiolate (C_{12}) on Au shows no sign of redox in the scanned potential window.[43,44] Therefore, the FcC_{11} junction provides a stable and voltage-programmable redox-active molecular channel.

Short-Term Synaptic Dynamics under Gate Pulses. To demonstrate artificial synaptic operation, we probed the

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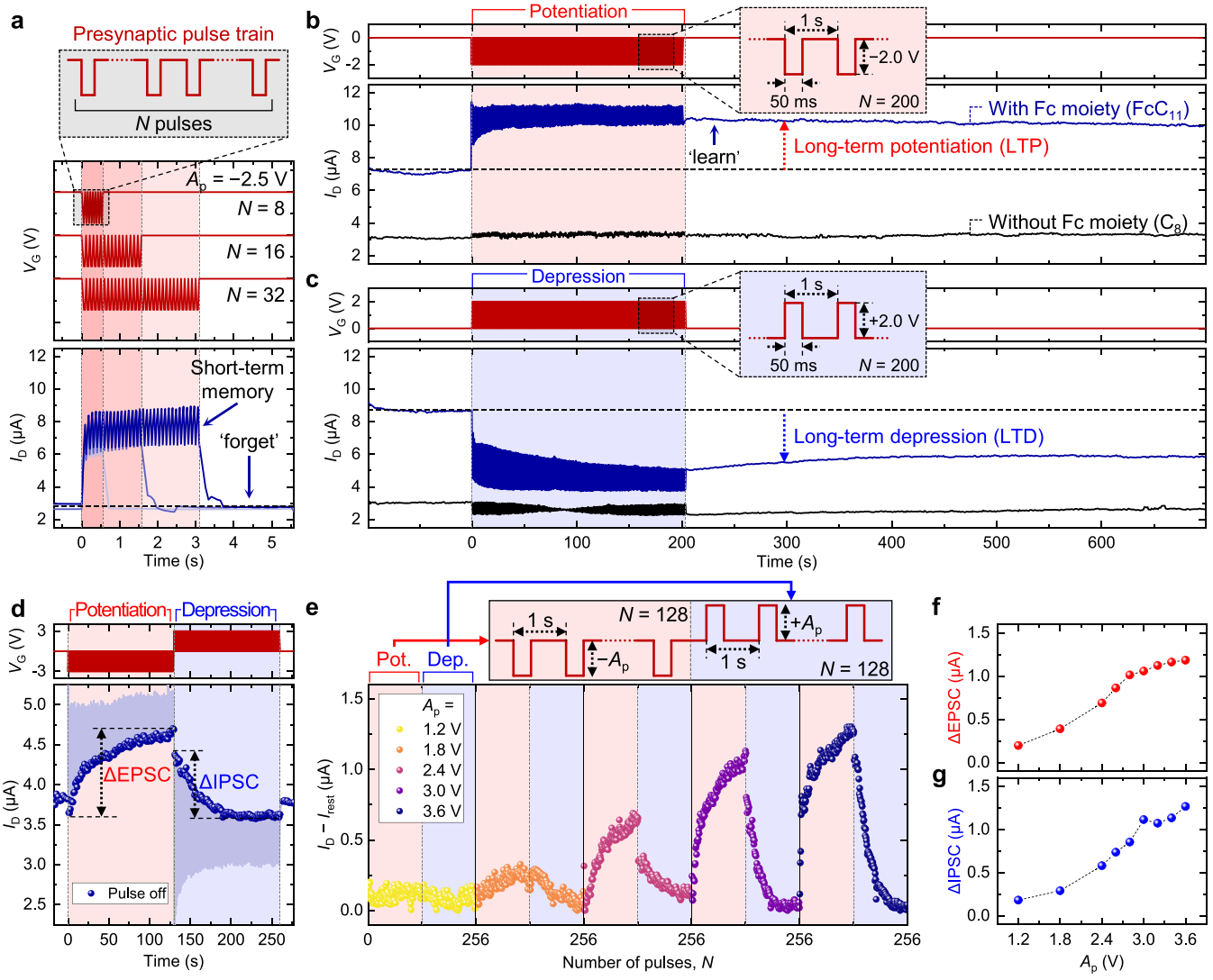

Figure 4. LTP/LTD characteristics. (a) Pulse train applied to the gate electrode with varying numbers of pulses N ranging from 8 to 32 (middle panel) and their zoomed-in illustration (top panel), with the corresponding postsynaptic current representing short-term memory characteristics (bottom panel). Representative (b) LTP and (c) LTD characteristics of the FcC_{11} transistor (blue) implemented by the pulse train illustrated in the top panel (red). Drain current of the C_8 transistor under the same potentiation pulse train (black) is compared, showing no LTP or LTD characteristics. (d) Sequential potentiation and depression pulse train (top panel) and resulting stepwise change of I_D (bottom panel), with blue shades showing I_D versus time, while blue symbols represent I_D measured between pulses (V_G = 0 V). (e) Change of I_D when potentiation and depression pulse train is serially applied, as illustrated in the top panel, with varying A_p, ranging from 1.2 to 3.6 V. Increase in (f) ΔEPSC and (g) ΔIPSC as a function of A_p, measured by pulse trains illustrated in the top panel of (e).

short-term plasticity (STP) with a single gate pulse (Figure 3a). A presynaptic pulse of duration t_p and amplitude A_p was applied to the gate (red-shaded area indicates the pulse duration in Figure 3a), while the postsynaptic response (I_D) was measured as a function of time at a constant bias V_D = 1.4 V. Prior to stimulation, the device maintains a steady rest current I_{rest}. A negative (positive) A_p instantly increases (decreases) I_D, followed by an exponential decay toward I_{rest}. We define this peak above I_{rest} as a postsynaptic spike and fitted it as $I_D(t) - I_{rest} = A_s \exp(-t/\tau)$ to obtain the postsynaptic spike amplitude A_s and the decay constant τ, where t is the time measured from the end of the pulse.[45,46]

At a fixed gate pulse amplitude of A_p = 2.5 V, increasing the pulse duration t_p from 5 to 30 ms facilitates both the postsynaptic spike amplitude A_s and its duration (Figure 3b). Longer pulses accumulate more ions in the ion-gel at the graphene interface, which enhances the electric double layer (EDL) formation. This results in a larger change in conductance achieved during the gate pulse and a longer decay time promoted by increased ionic population at the graphene interface. Separately, raising the pulse amplitude A_p from −0.5 to −2.5 V at a fixed duration (t_p = 50 ms) produces larger spikes (Figure 3c), implying enhanced ion migration and the resulting gate field. In short, t_p primarily controls the extent of EDL formation (and thus the recovery time), whereas A_p mainly amplifies the gating response observed within the measurement window. These trends are summarized in Figure 3d–f. The spike amplitude A_s grows with t_p and approaches a saturation value of ∼1.6 μA (Figure 3d). In contrast, the relaxation time τ increases with t_p without clear saturation for up to 30 ms (Figure 3e). Noting that the full rearrangement of ion-gel is slow (up to ∼10 s),[47,48] the saturating behavior of A_s and nonsaturating behavior of τ imply two time scales: short pulses quickly build the near-graphene ionic layer (setting A_s),

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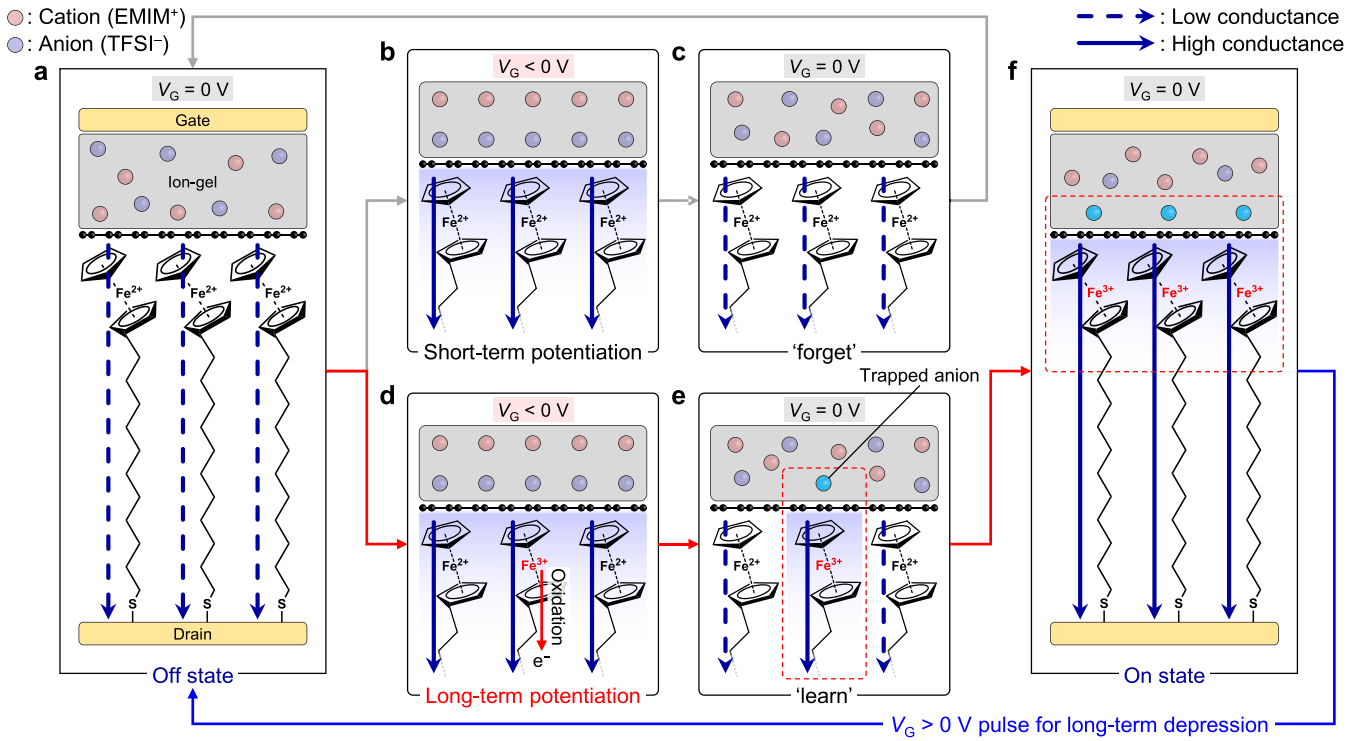

Figure 5. Suggested mechanisms of STP (gray arrows), LTP (red arrows), and LTD (blue arrow). (a) Initially, at V_G = 0 V, the ferrocene moiety is in a low conductance state (dashed blue arrows), and the ions in the ion-gel show no ordering. (b) When negative V_G is applied, the anion layer is formed near the graphene surface, gating up the HOMO level and thus the junction is at a high conductance level (solid blue arrows). (c) As the V_G returns to zero, the ions diffuse and the gate field vanishes, returning to the low conductance state; thus, the potentiation is short-term. (d) A repeated application of a potentiation pulse induces rearrangement of ionic layers, while an Fc moiety can undergo oxidation. (e) Anions can be placed near Fc^+, trapped by Coulomb interaction even after V_G is set to zero, resulting in a steady gate field and high conductance of the molecular channel (solid blue arrow). (f) Saturation in formation of Fc^+−anion pairs gives potentiated I_D.

whereas slower, deeper ionic reorganization in the ion-gel controls the subsequent decay (increasing τ).[48] Finally, A_s scales linearly with A_p at fixed t_p = 50 ms (Figure 3f), providing an effective parameter to program the spike amplitude.

Figure 3g–i demonstrates paired-pulse facilitation (PPF), a key feature of STP. A pair of two identical gate pulses separated by an interpulse interval Δt brings out the first postsynaptic spike with an amplitude of A_{s1} and the second postsynaptic spike with an amplitude of A_{s2} that exceeds A_{s1} when the Δt is short (Figure 3g). This facilitation arises because anions accumulated near the graphene interface during the first pulse cannot fully disperse within $\Delta t \sim 100$ ms. The residual ionic population promotes a denser accumulation upon the second pulse, strengthening the effective gate field. Representative traces at $A_p = -2.5$ V and t_p = 50 ms show that the difference between A_{s1} and A_{s2} diminishes as Δt increases (Figure 3h), indicating gradual "forgetting". The PPF index, defined as A_{s2}/A_{s1}, decays with Δt and is well described by a two-phase exponential decay model $C_1 e^{-\Delta t/\tau_1} + C_2 e^{-\Delta t/\tau_2}$ (Figure 3i), yielding τ_1 = 54 ms and τ_2 = 200 ms.[46] These two time scales are consistent with a fast decaying EDL component and a slower diffusive component.[48] Moreover, they fall within canonical STP windows in biological synapses, in which their facilitation typically decays over tens of milliseconds, while slower components last from hundreds of milliseconds to seconds, supporting the neuromorphic relevance of our device response.[26] Consequently, the spike size and the short-term memory time scale of our ion-gel/graphene FcC_{11} transistor can be tuned independently via the pulse amplitude A_p, pulse width t_p, and interpulse interval Δt, which are all key features for STP.

Programmable Short- and Long-Term Plasticity. We then investigated the programming of synaptic states in our molecular transistor using various designated pulse trains and characterized their temporal dynamics. Figure 4a summarizes the short-term memory regime. We applied trains of identical negative gate pulses (amplitude $A_p = -2.5$ V and duration t_p = 50 ms; the pulse windows are shaded red) and monitored I_D over t while holding V_D constant. Prior to stimulation, I_D is steady at I_{rest} (horizontal dashed line). As the number of pulses N increases from 8 to 16 to 32, the postsynaptic spikes grow larger, which is evidence that successive pulses accumulate interfacial charge and temporarily enhance the channel conductance. However, the enhancement is volatile. Once the pulse train ends, I_D decays back to I_{rest} within ~1 s. The device "forgets" the recent history with an exponential relaxation, which is a characteristic of an STP.

However, for a larger number of pulses, the potentiation is retained for longer than hundreds of seconds, as described in Figure 4b. The pulse train of N = 200 pulses (with $A_p = -2.0$ V, t_p = 50 ms, and a 1 s period) produces long-term potentiation (LTP) in the FcC_{11} device (blue trace). Here, we plot I_D as a function of t so that the retention can be seen clearly. After the pulse train, the current remains elevated for hundreds of seconds with negligible decay, i.e., a nonvolatile memory state. In contrast, an otherwise identical control C_8 junction without the Fc moiety shows no persistent increase (black trace). This comparison indicates that redox activity in the Fc moiety is necessary to stabilize the potentiated state

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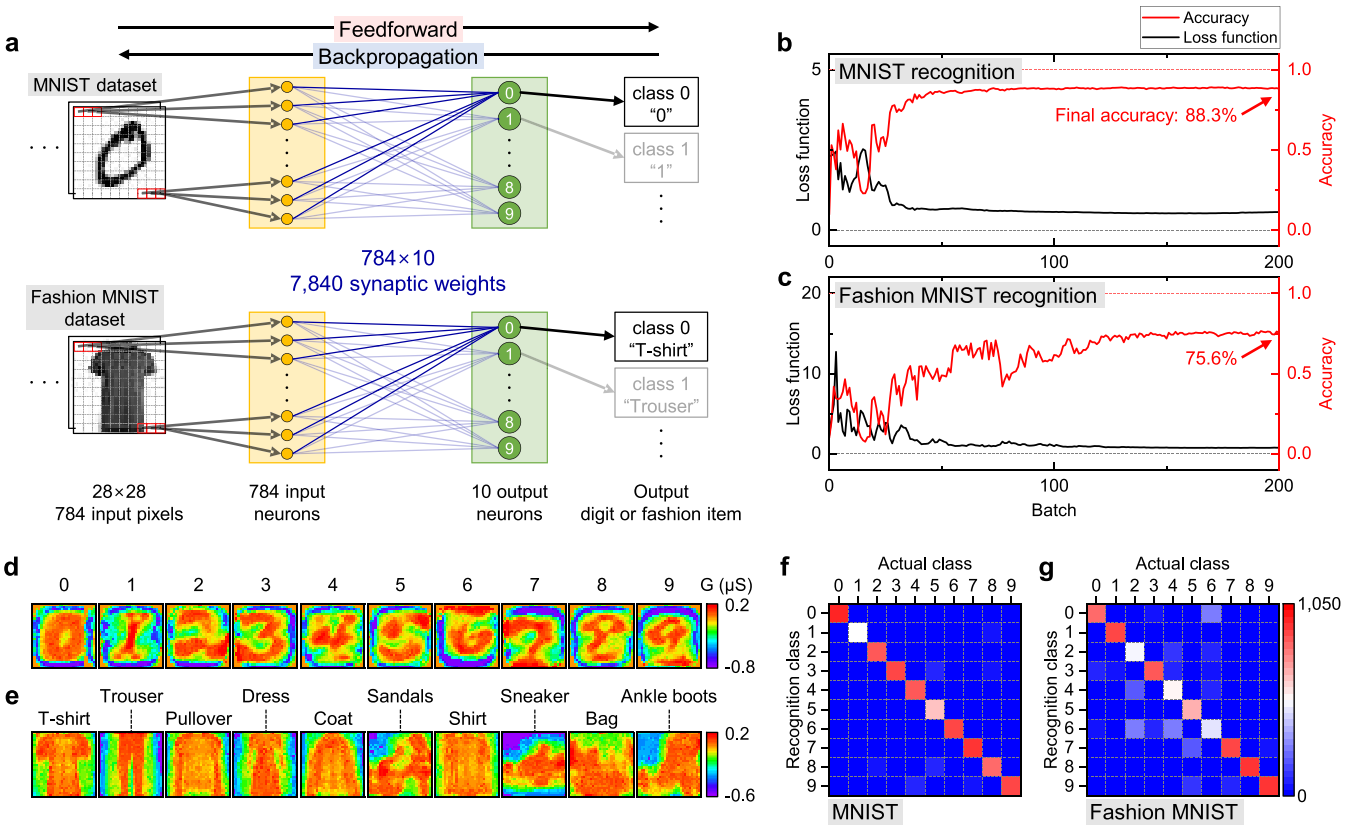

Figure 6. MNIST and Fashion MNIST simulations. (a) Schematic illustration of ANNs simulated in this study, comprising 784 input neurons and 10 output neurons without a hidden layer, with all synaptic weights between neurons are represented by the conductance of FcC_{11} transistors. Total accuracy (red) and loss function (black) for the (b) MNIST test set and (c) Fashion MNIST test set, achieved by ANNs as a function of the number of batches (a total of 200 batches). Synaptic weights between input neurons and each output neuron (d) from digits and (e) fashion items, which shows the typical shape of each class. The confusion matrix between recognition and actual classes for (f) MNIST and (g) Fashion MNIST simulations, showing pronounced diagonal elements.

under this pulse train condition. For practical operation, the synaptic state should be erasable and bidirectionally programmable. Figure 4c demonstrates this reversibility. A sequence of positive pulses (A_p = +2.0 V, t_p = 50 ms, 1 s period, and N = 200) drives the FcC_{11} device back toward I_{rest}, yielding long-term depression (LTD) (blue trace). The C_8 control device again shows no significant long-term change (black trace).

With this gate tunability, we demonstrated the transition between LTP and LTD of I_D at V_D = 1.5 V, achieved by 128 negative pulses (red-shaded region) and 128 positive pulses (blue-shaded region). Note that each blue dot represents the available analog state that can be utilized as synaptic weights. The net change accumulated over the entire potentiation and depression pulse train is denoted ΔEPSC (excitatory postsynaptic current) and ΔIPSC (inhibitory postsynaptic current), respectively. Notably, a square-wave input in gate voltage with the same total on-time (t_p = 6.4 and 10 s, for Figure 4b–e, each) resulted in volatile responses, failing to implement LTP (Figure S30). This implies that the dynamic change of gate voltage facilitates LTP, compared with the static gate input.

The pulse amplitude dependence of these states is mapped in Figure 4e. Keeping t_p = 50 ms, period = 1 s, and pulse count per block at N = 128, we swept $|A_p|$ from 1.2 to 3.6 V (red segments for LTP and blue segments for LTD). Clearly, $I_D - I_{rest}$ increases monotonically with $|A_p|$, enabling graded multilevel states. The extracted ΔEPSC and ΔIPSC are plotted versus $|A_p|$ in Figures 4f and g, respectively, showing a linear dependence on A_p. The LTP and LTD properties of FcC_{11} transistors including their memristive behavior and tunability of states via A_p are advantageous for learning because they provide a practical way to set the junction conductance to the desired value.

Mechanism of Short- and Long-Term Plasticity. The synaptic behaviors of FcC_{11} transistors can be comprehended based on a redox-assisted ionic mechanism at the ion-gel/graphene FcC_{11} interface. In the initial unbiased state (V_G = 0 V, Figure 5a), $EMIM^+$ and $TFSI^-$ ions are in equilibrium within the PS-PMMA-PS gel, and the FcC_{11} monolayer is predominantly neutral ferrocene (Fc, Fe^{2+}). Because no transverse field penetrates the monolayer graphene, the junction conducts at I_{rest} (low conductance state).

A negative gate pulse (V_G < 0) induces accumulation of $TFSI^-$ at the graphene surface, forming an electric field that penetrates the atomically thin graphene (Figure 5b). The resulting electrostatic shift raises the Fc HOMO toward the transport window (see the Supporting Information, Section 6),[38,39] transiently enhancing the current (postsynaptic spike, high conductance state). When the gate returns to zero, interfacial anions relax by diffusion on a time scale of subsecond to second[48,49] and the current decays exponentially back to I_{rest} (Figure 5c), resulting in volatile short-term potentiation. Because the ion-gel exhibits slow structural kinetics (up to ~10 s),[47,48] paired pulses with short Δt encounter residual anions that promote faster, denser

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accumulation during the second pulse, yielding PPF as in Figure 3g–i.

With repeated negative gate pulses, a fraction of Fc units oxidize to ferrocenium (Fc^+, Fe^{3+}) near the graphene interface (Figure 5d). Oppositely charged $TFSI^-$ is then electrostatically trapped across the graphene by Coulomb attraction to Fc^+, even after the gate voltage is set to zero (Figure 5e, red dashed box), resulting in a fraction of FcC_{11} molecules remaining in the high conductance state. The interfacial binding of ions due to the charge on the other side of monolayer graphene is repeatedly reported for charged defects in oxides[50,51] or ferroelectric overlayers.[52] The trapping of $TFSI^-$ on graphene near Fc^+ is also supported by the reported affinity of $TFSI^-$ for bare graphene via van der Waals interactions.[53] This anion–Fc^+ pair may occur after applying about 50 potentiation pulses (Supporting Information, Figure S26), while 32 pulses were insufficient to achieve long-term potentiation (Figure 4a). As more pulses are applied, the increase in the number of trapped anions results in a nonvolatile interfacial field that maintains a high conductance state with extended retention (Figure 5f). The volatile response to the long, single pulses (with t_p = 6.4, 10 s) in Figure S30 (Supporting Information) is also consistent with this mechanism. While the pulse train induces rearrangement of anions by altering the gate field, a square-wave gate voltage results in a static electric field, which reduces the possibility for an anion to find a trap site to form an anion–Fc^+ pair. More detailed discussions on the comparison between a single square-wave gate voltage and the pulse train input are provided in the Supporting Information (Section 8). This redox-dependent mechanism is supported by the absence of LTP characteristics in the control device with a redox-inactive alkyl (C_8) SAM under identical gating (Figure 4b). A quantitative analysis of the relationship between the population of Fc^+ that forms a pair with $TFSI^-$ is presented in the Supporting Information (Section 10), which reveals that the gating effect induced by the nonvolatile field shifts HOMO upward up to about 0.1 eV.

Reversibility and polarity asymmetry follow naturally from this picture. A positive pulse train ($V_G > 0$) promotes detrapping and removal of interfacial anions, erasing the residual field and returning the device toward I_{rest} (long-term depression; Figure 4c). Because the accessible Fc redox states in our junction are neutral Fc and cationic Fc^+ (no stable anionic state), an analogous route based on persistent cation trapping is not available; accordingly, we do not observe conductance that remains below the original baseline after positive programming. For both LTP and LTD processes, changes in the population of the anion–Fc^+ pair and corresponding drain current states are presented in the Supporting Information (Section 10).

MNIST and Fashion MNIST Classification Using FcC_{11} Synaptic Molecular Transistors. To demonstrate system-level function, we simulated ANN-based learning on handwritten-digit recognition (MNIST) and fashion-item recognition (Fashion MNIST) using the synaptic characteristics of FcC_{11} devices. For both simulations, ANNs were configured as the same structure, which maps the 784 input neurons (from 28 × 28 pixels) directly into 10 output neurons without hidden layers, yielding 784 × 10 = 7840 synaptic weights (Figure 6a). The feedforward process (or forward propagation) results in the conversion of an image into 10 output values, and the class of the image is determined as the class corresponding to the output neuron with the maximum value. Learning of ANN is implemented by conventional batch mode back-propagation of errors to minimize the cross-entropy loss function based on the softmax of output neurons. Each weight was implemented as a differential pair of FcC_{11} synaptic devices, which provides a straightforward method for updating weights only with potentiation pulses.[54−58] For simulations, a total of 128 steps of the conductance values of FcC_{11} synaptic devices under potentiation pulses with A_p = −3.6 V, t_p = 50 ms, with a period of 1 s (see Figure 4e), were used. This pulse condition with relatively large A_p is advantageous for the large dynamic range in conductance, which promotes effective learning. Details of the simulation setup are provided in the Experimental Section and in the Supporting Information (Section 11).

Each model was trained for one epoch on MNIST or Fashion MNIST (200 batches of 300 images). Figures 6b (MNIST) and 6c (Fashion MNIST) track the evolution of accuracy (red) and the loss function (black) versus the trained number of batches, respectively, tested by 10,000 test set images in each step of batch learning. The accuracy increases with the learning process, reaching 88.3 and 75.6% after 200 batches, respectively. The large fluctuation in accuracy for the first few tens of batch learnings is attributed to the rapid change of conductance of FcC_{11} synaptic devices for the initial few pulses, which results in overshooting in the update of weights. As the weights update with batches, the number of pulses applied to FcC_{11} devices increases, and the increment between conductance states becomes stabilized (Figure 4e), giving slower yet steady learning. Also, the loss function decreases well.

The learned weight maps are presented in Figures 6d (MNIST) and 6e (fashion MNIST), with the labels for each class. Positively (negatively) updated pixels are indicated as red (purple). It is notable that the red regions correspond to the shape of the digit or fashion item, while the purple regions represent the pixels absent in the given class but present in other classes. The confusion matrices for MNIST (Figure 6f) and fashion MNIST (Figure 6g) are also depicted. In Figure 6g, the class numbers indicate the fashion items in the order presented in Figure 6e. For both simulations, ANNs were trained well with predominant diagonal components in confusion matrices. All these results, including accuracy, synaptic weights, and confusion matrices, confirm the learning capability for our molecular artificial synapses.

CONCLUSIONS

In summary, this study demonstrated the redox-induced synaptic device in the form of a molecular transistor. The presynaptic pulse was implemented by a gate pulse, and the corresponding change of drain current was regarded as an artificial postsynaptic spike. The main conduction mechanism through the device was attributed to a HOMO-mediated redox process in the ferrocene moiety. An intensive and long presynaptic (gate) pulse enhances the drain current, imitating postsynaptic spikes on time scales of 10–100 ms, similar to those of biological synapses. This short-term memory is observed for many pulses, up to a maximum of 32. However, for more repeated potentiating pulses, a nondecaying, long-term potentiation of postsynaptic current was achieved. Long-term potentiated drain current can also be depressed by depression pulses, completing the set of artificial learning and forgetting. The mechanism for short-term and long-term potentiation was attributed to the slow kinetics of the ion and its Coulomb interactions with positively charged ferrocenium,

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respectively. Lastly, the ANN of a two-layer structure with its neurons connected by a molecular synaptic device was simulated to solve the digit classifying problem for the MNIST data set, yielding an accuracy of 88.3%. This work demonstrates the potential for developing molecular-based neuromorphic electronics.

EXPERIMENTAL SECTION

Device Fabrication and Electrical Characterization. P-type silicon substrates and glass substrates were cleaned by sonication in acetone, 2-propanol, and deionized water for 10 min each, followed by N_2 drying. A 50 nm thick Au layer was deposited on silicon substrates through a shadow mask using electron-beam evaporation (KVE-2004L, Korea Vacuum Tech.). Glass substrates were surface-treated with UV exposure for 10 min, after which optical adhesive (OA) (Norland, 61) was dispensed onto the Au/Si substrate and covered with the glass substrate. After curing OA under UV for an hour, the Au/OA/glass substrate was template-stripped from the silicon substrate using the razor blade. On this substrate, insulating PR wall structure was patterned by photolithography and holes with radius 2 μm were defined to expose Au surfaces. A 5 mM ethanol solution of FcC_{11} was prepared, and the substrate was immersed for 24 h under a N_2 atmosphere to form FcC_{11} SAMs on the exposed Au region. A monolayer of graphene grown with chemical vapor deposition on Cu foil was purchased from Graphene Square Inc. and wet-transferred onto the substrate as the top electrode. An ion-gel composed of a PS-PMMA-PS triblock copolymer and [EMIM][TFSI] in ethyl acetate (1:9:90, w/w/w) was drop-cast onto the graphene electrode and dried under vacuum. The electrical characteristics of the devices were measured with Source Measure Unit and Pulse Measure Unit modules of the semiconductor parameter analyzer (Keithley 4200-SCS) in a vacuum probe station (MS TECH). Cyclic voltammetry was performed using a potentiostat (SP-200, BioLogic) with a three-electrode configuration with Ag/AgCl (3 M NaCl) as the reference electrode.

MNIST and Fashion MNIST Simulation. Training and test sets of MNIST and Fashion MNIST were used as provided without modification from their original form.[59] A total of 60,000 training images were divided into 200 batches, and the ANN with one input layer of 784 input neurons and one output layer of 10 output neurons was simulated. The training was simulated with batch gradient back-propagation based on the cross-entropy loss function.[58,60,61] Neurons in each layer are connected to the other layer with synaptic weight described by the difference in conductance of two synaptic devices, as suggested by Prezioso et al.[54] Thus, updating the positive or negative weight was emulated by potentiating a "positive" synaptic device or its "negative pair". 128 steps of conductance of synaptic devices were used in simulation, and for each batch gradient, the weight update was performed by only one potentiating one of each differential pair of synaptic devices, depending on the sign of the desired back-propagation. Input signals were normalized in the 0 to 1 scale, and the output value was normalized by a factor of 2 μS before getting softmax. More detailed methods including flowchart (Figure S38) can be found in the Supporting Information (Section 11).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.5c17016.

Additional details on the materials and fabrication process, electrical characterizations of FcC_{11} devices and their fitting to Marcus theory, and discussions on the activation energy and MNIST simulations (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Aviram, A.; Ratner, M. A. Molecular Rectifiers. *Chem. Phys. Lett.* **1974**, *29* (2), 277−283.

(2) Chen, X.; Roemer, M.; Yuan, L.; Du, W.; Thompson, D.; del Barco, E.; Nijhuis, C. A. Molecular Diodes with Rectification Ratios Exceeding 105 Driven by Electrostatic Interactions. *Nat. Nanotechnol.* **2017**, *12* (8), 797−803.

(3) Wang, K.; Meyhofer, E.; Reddy, P. Thermal and Thermoelectric Properties of Molecular Junctions. *Adv. Funct. Mater.* **2020**, *30* (8), No. 1904534.

(4) Bueno, P. R.; Davis, J. J. Charge Transport and Energy Storage at the Molecular Scale: From Nanoelectronics to Electrochemical Sensing. *Chem. Soc. Rev.* **2020**, *49* (21), 7505−7515.

(5) He, P.; Jang, J.; Kang, H.; Yoon, H. J. Thermoelectricity in Molecular Tunnel Junctions. *Chem. Rev.* **2025**, *125* (5), 2953−3004.
(6) Schirm, C.; Matt, M.; Pauly, F.; Cuevas, J. C.; Nielaba, P.; Scheer, E. A Current-Driven Single-Atom Memory. *Nat. Nanotechnol.* **2013**, *8* (9), 645−648.
(7) Song, H.; Kim, Y.; Jang, Y. H.; Jeong, H.; Reed, M. A.; Lee, T. Observation of Molecular Orbital Gating. *Nature* **2009**, *462* (7276), 1039−1043.
(8) Sasao, K.; Azuma, Y.; Kaneda, N.; Hase, E.; Miyamoto, Y.; Majima, Y. Observation of Current Modulation through Self-Assembled Monolayer Molecule in Transistor Structure. *Jpn. J. Appl. Phys.* **2004**, *43* (3A), No. L337.
(9) Richter, S.; Mentovich, E.; Elnathan, R. Realization of Molecular-Based Transistors. *Adv. Mater.* **2018**, *30* (41), No. 1706941.
(10) Schwarz, F.; Kastlunger, G.; Lissel, F.; Egler-Lucas, C.; Semenov, S. N.; Venkatesan, K.; Berke, H.; Stadler, R.; Lörtscher, E. Field-Induced Conductance Switching by Charge-State Alternation in Organometallic Single-Molecule Junctions. *Nat. Nanotechnol.* **2016**, *11* (2), 170−176.
(11) Trasobares, J.; Martín-Romano, J. C.; Khaliq, M. W.; Ruiz-Gómez, S.; Foerster, M.; Niño, M. Á.; Pedraz, P.; Dappe, Y. J.; de Ory, M. C.; García-Pérez, J.; Acebrón, M.; Osorio, M. R.; Magaz, M. T.; Gomez, A.; Miranda, R.; Granados, D. Hybrid Molecular Graphene Transistor as an Operando and Optoelectronic Platform. *Nat. Commun.* **2023**, *14* (1), No. 1381.
(12) Indiveri, G.; Liu, S.-C. Memory and Information Processing in Neuromorphic Systems. *Proc. IEEE* **2015**, *103* (8), 1379−1397.
(13) Lee, Y.; Oh, J. Y.; Lee, T.-W. Neuromorphic Skin Based on Emerging Artificial Synapses. *Adv. Mater. Technol.* **2022**, *7* (12), No. 2200193.
(14) Han, H.; Yu, H.; Wei, H.; Gong, J.; Xu, W. Recent Progress in Three-Terminal Artificial Synapses: From Device to System. *Small* **2019**, *15* (32), No. 1900695.
(15) Chen, S.; Zhang, T.; Tappertzhofen, S.; Yang, Y.; Valov, I. Electrochemical-Memristor-Based Artificial Neurons and Synapses—Fundamentals, Applications, and Challenges. *Adv. Mater.* **2023**, *35* (37), No. 2301924.
(16) Dai, S.; Zhao, Y.; Wang, Y.; Zhang, J.; Fang, L.; Jin, S.; Shao, Y.; Huang, J. Recent Advances in Transistor-Based Artificial Synapses. *Adv. Funct. Mater.* **2019**, *29* (42), No. 1903700.
(17) Wu, C.; Kim, T. W.; Choi, H. Y.; Strukov, D. B.; Yang, J. J. Flexible Three-Dimensional Artificial Synapse Networks with Correlated Learning and Trainable Memory Capability. *Nat. Commun.* **2017**, *8* (1), No. 752.
(18) Yu, S.; Wu, Y.; Jeyasingh, R.; Kuzum, D.; Wong, H.-S. P. An Electronic Synapse Device Based on Metal Oxide Resistive Switching Memory for Neuromorphic Computation. *IEEE Trans. Electron Devices* **2011**, *58* (8), 2729−2737.
(19) Chang, T.; Jo, S.-H.; Kim, K.-H.; Sheridan, P.; Gaba, S.; Lu, W. Synaptic Behaviors and Modeling of a Metal Oxide Memristive Device. *Appl. Phys. A: Mater. Sci. Process.* **2011**, *102* (4), 857−863.
(20) Yang, C. S.; Shang, D. S.; Liu, N.; Shi, G.; Shen, X.; Yu, R. C.; Li, Y. Q.; Sun, Y. A Synaptic Transistor Based on Quasi-2D Molybdenum Oxide. *Adv. Mater.* **2017**, *29* (27), No. 1700906.
(21) Jiang, J.; Hu, W.; Xie, D.; Yang, J.; He, J.; Gao, Y.; Wan, Q. 2D Electric-Double-Layer Phototransistor for Photoelectronic and Spatiotemporal Hybrid Neuromorphic Integration. *Nanoscale* **2019**, *11* (3), 1360−1369.
(22) Arnold, A. J.; Razavieh, A.; Nasr, J. R.; Schulman, D. S.; Eichfeld, C. M.; Das, S. Mimicking Neurotransmitter Release in Chemical Synapses via Hysteresis Engineering in MoS2 Transistors. *ACS Nano* **2017**, *11* (3), 3110−3118.
(23) Yang, Y.; Huang, R. Probing Memristive Switching in Nanoionic Devices. *Nat. Electron.* **2018**, *1* (5), 274−287.
(24) Sun, J.; Fu, Y.; Wan, Q. Organic Synaptic Devices for Neuromorphic Systems. *J. Phys. Appl. Phys.* **2018**, *51* (31), No. 314004.
(25) Li, S.; Zeng, F.; Chen, C.; Liu, H.; Tang, G.; Gao, S.; Song, C.; Lin, Y.; Pan, F.; Guo, D. Synaptic Plasticity and Learning Behaviours Mimicked through Ag Interface Movement in an Ag/Conducting Polymer/Ta Memristive System. *J. Mater. Chem. C* **2013**, *1* (34), 5292−5298.
(26) Zucker, R. S.; Regehr, W. G. Short-Term Synaptic Plasticity. *Annu. Rev. Physiol.* **2002**, *64* (64), 355−405.
(27) Di Filippo, M.; Picconi, B.; Tantucci, M.; Ghiglieri, V.; Bagetta, V.; Sgobio, C.; Tozzi, A.; Parnetti, L.; Calabresi, P. Short-Term and Long-Term Plasticity at Corticostriatal Synapses: Implications for Learning and Memory. *Behav. Brain Res.* **2009**, *199* (1), 108−118.
(28) Zhang, Q.; Wang, Y.; Nickle, C.; Zhang, Z.; Leoncini, A.; Qi, D.-C.; Sotthewes, K.; Borrini, A.; Zandvliet, H. J. W.; del Barco, E.; Thompson, D.; Nijhuis, C. A. Molecular Switching by Proton-Coupled Electron Transport Drives Giant Negative Differential Resistance. *Nat. Commun.* **2024**, *15* (1), No. 8300.
(29) Wang, Y.; Zhang, Q.; Astier, H. P. A. G.; Nickle, C.; Soni, S.; Alami, F. A.; Borrini, A.; Zhang, Z.; Honnigfort, C.; Braunschweig, B.; Leoncini, A.; Qi, D.-C.; Han, Y.; del Barco, E.; Thompson, D.; Nijhuis, C. A. Dynamic Molecular Switches with Hysteretic Negative Differential Conductance Emulating Synaptic Behaviour. *Nat. Mater.* **2022**, *21* (12), 1403−1411.
(30) Goswami, S.; Pramanick, R.; Patra, A.; Rath, S. P.; Foltin, M.; Ariando, A.; Thompson, D.; Venkatesan, T.; Goswami, S.; Williams, R. S. Decision Trees within a Molecular Memristor. *Nature* **2021**, *597* (7874), 51−56.
(31) Zhang, Y.; Liu, L.; Tu, B.; Cui, B.; Guo, J.; Zhao, X.; Wang, J.; Yan, Y. An Artificial Synapse Based on Molecular Junctions. *Nat. Commun.* **2023**, *14* (1), No. 247.
(32) Ham, S.; Jang, J.; Koo, D.; Gi, S.; Kim, D.; Jang, S.; Kim, N. D.; Bae, S.; Lee, B.; Lee, C.-H.; Wang, G. Artificial Neuromodulator−Synapse Mimicked by a Three-Terminal Vertical Organic Ferroelectric Barristor for Fast and Energy-Efficient Neuromorphic Computing. *Nano Energy* **2024**, *124*, No. 109435.
(33) Huh, W.; Lee, D.; Jang, S.; Kang, J. H.; Yoon, T. H.; So, J.-P.; Kim, Y. H.; Kim, J. C.; Park, H.-G.; Jeong, H. Y.; Wang, G.; Lee, C.-H. Heterosynaptic MoS_2 Memtransistors Emulating Biological Neuromodulation for Energy-Efficient Neuromorphic Electronics. *Adv. Mater.* **2023**, *35* (24), No. 2211525.
(34) Choi, S.; Jang, J.; Kim, M. S.; Kim, N. D.; Kwag, J.; Wang, G. Flexible Neural Network Realized by the Probabilistic SiOx Memristive Synaptic Array for Energy-Efficient Image Learning. *Adv. Sci.* **2022**, *9* (11), No. 2104773.
(35) Yan, X.; Qian, J. H.; Sangwan, V. K.; Hersam, M. C. Progress and Challenges for Memtransistors in Neuromorphic Circuits and Systems. *Adv. Mater.* **2022**, *34* (48), No. 2108025.
(36) Keane, Z. K.; Ciszek, J. W.; Tour, J. M.; Natelson, D. Three-Terminal Devices to Examine Single-Molecule Conductance Switching. *Nano Lett.* **2006**, *6* (7), 1518−1521.
(37) Jia, C.; Grace, I. M.; Wang, P.; Almeshal, A.; Huang, Z.; Wang, Y.; Chen, P.; Wang, L.; Zhou, J.; Feng, Z.; Zhao, Z.; Huang, Y.; Lambert, C. J.; Duan, X. Redox Control of Charge Transport in Vertical Ferrocene Molecular Tunnel Junctions. *Chem* **2020**, *6* (5), 1172−1182.
(38) Jia, C.; Famili, M.; Carlotti, M.; Liu, Y.; Wang, P.; Grace, I. M.; Feng, Z.; Wang, Y.; Zhao, Z.; Ding, M.; Xu, X.; Wang, C.; Lee, S.-J.; Huang, Y.; Chiechi, R. C.; Lambert, C. J.; Duan, X. Quantum Interference Mediated Vertical Molecular Tunneling Transistors. *Sci. Adv.* **2018**, *4* (10), No. eaat8237.
(39) Kim, D.; Lee, H.; Song, M.; Nam, J.; Lee, C.; Woo, J.; Jang, J.; Jeong, M.; Yeo, H.; Lee, R.-G.; Park, E.; Choi, H.; Kim, Y.-H.; Kang, K.; Lee, T. Enhanced Gating Efficiency in Vertical Mixed Molecular Transistors with Deep Orbital Level. *Sci. Adv.* **2025**, *11* (25), No. eadt3603.
(40) Cho, J. H.; Lee, J.; Xia, Y.; Kim, B.; He, Y.; Renn, M. J.; Lodge, T. P.; Frisbie, C. D. Printable Ion-Gel Gate Dielectrics for Low-Voltage Polymer Thin-Film Transistors on Plastic. *Nat. Mater.* **2008**, *7* (11), 900−906.
(41) Yuan, L.; Wang, L.; Garrigues, A. R.; Jiang, L.; Annadata, H. V.; Anguera Antonana, M.; Barco, E.; Nijhuis, C. A. Transition from Direct to Inverted Charge Transport Marcus Regions in Molecular

https://doi.org/10.1021/acsnano.5c17016
ACS Nano 2026, 20, 1170−1180

Junctions via Molecular Orbital Gating. *Nat. Nanotechnol.* **2018**, *13* (4), 322−329.
(42) Nijhuis, C. A.; Reus, W. F.; Barber, J. R.; Dickey, M. D.; Whitesides, G. M. Charge Transport and Rectification in Arrays of SAM-Based Tunneling Junctions. *Nano Lett.* **2010**, *10* (9), 3611−3619.
(43) Elgrishi, N.; Rountree, K. J.; McCarthy, B. D.; Rountree, E. S.; Eisenhart, T. T.; Dempsey, J. L. A Practical Beginner's Guide to Cyclic Voltammetry. *J. Chem. Educ.* **2018**, *95* (2), 197−206.
(44) Chidsey, C. E. D. Free Energy and Temperature Dependence of Electron Transfer at the Metal-Electrolyte Interface. *Science* **1991**, *251* (4996), 919−922.
(45) Kirk, M. E.; Meredith, F. L.; Benke, T. A.; Rennie, K. J. AMPA Receptor-Mediated Rapid EPSCs in Vestibular Calyx Afferents. *J. Neurophysiol.* **2017**, *117* (6), 2312−2323.
(46) Häusser, M.; Roth, A. Estimating the Time Course of the Excitatory Synaptic Conductance in Neocortical Pyramidal Cells Using a Novel Voltage Jump Method. *J. Neurosci.* **1997**, *17* (20), 7606−7625.
(47) Uysal, A.; Zhou, H.; Feng, G.; Lee, S. S.; Li, S.; Fenter, P.; Cummings, P. T.; Fulvio, P. F.; Dai, S.; McDonough, J. K.; Gogotsi, Y. Structural Origins of Potential Dependent Hysteresis at the Electrified Graphene/Ionic Liquid Interface. *J. Phys. Chem. C* **2014**, *118* (1), 569−574.
(48) Cho, J. H.; Lee, J.; He, Y.; Kim, B. S.; Lodge, T. P.; Frisbie, C. D. High-Capacitance Ion Gel Gate Dielectrics with Faster Polarization Response Times for Organic Thin Film Transistors. *Adv. Mater.* **2008**, *20* (4), 686−690.
(49) Lee, J.; Kaake, L. G.; Cho, J. H.; Zhu, X.-Y.; Lodge, T. P.; Frisbie, C. D. Ion Gel-Gated Polymer Thin-Film Transistors: Operating Mechanism and Characterization of Gate Dielectric Capacitance, Switching Speed, and Stability. *J. Phys. Chem. C* **2009**, *113* (20), 8972−8981.
(50) Mišković, Z. L.; Sharma, P.; Goodman, F. O.; et al. Ionic Screening of Charged Impurities in Electrolytically Gated Graphene. *Phys. Rev. B* **2012**, *86* (11), No. 115437, DOI: 10.1103/PhysRevB.86.115437.
(51) Chen, F.; Xia, J.; Tao, N. Ionic Screening of Charged-Impurity Scattering in Graphene. *Nano Lett.* **2009**, *9* (4), 1621−1625.
(52) Ma, C.; Lu, R.; Hu, G.; Han, J.; Liu, M.; Li, J.; Wu, J. Detecting Electric Dipoles Interaction at the Interface of Ferroelectric and Electrolyte Using Graphene Field Effect Transistors. *ACS Appl. Mater. Interfaces* **2017**, *9* (4), 4244−4252.
(53) Zhang, Y.; Hu, G.; Gong, M.; Alamri, M.; Ma, C.; Liu, M.; Wu, J. Z. Lateral Graphene p−n Junctions Realized by Nanoscale Bipolar Doping Using Surface Electric Dipoles and Self-Organized Molecular Anions. *Adv. Mater. Interfaces* **2019**, *6* (1), No. 1801380.
(54) Prezioso, M.; Merrikh-Bayat, F.; Hoskins, B. D.; Adam, G. C.; Likharev, K. K.; Strukov, D. B. Training and Operation of an Integrated Neuromorphic Network Based on Metal-Oxide Memristors. *Nature* **2015**, *521* (7550), 61−64.
(55) Eo, J. S.; Shin, J.; Jeon, T.; Jang, J.; Wang, G. Tilt-Engineered Molecular-Scale Selector for Enhanced Learning in Artificial Neural Networks. *Adv. Funct. Mater.* **2024**, *34* (16), No. 2311103.
(56) Gao, K.; Sun, B.; Yang, B.; Cao, Z.; Cui, Y.; Wang, M.; Kong, C.; Zhou, G.; Luo, S.; Chen, X.; Shao, J. An Organic Artificial Synaptic Memristor for Neuromorphic Computing. *Appl. Mater. Today* **2025**, *43*, No. 102628.
(57) Ham, S.; Kang, M.; Jang, S.; Jang, J.; Choi, S.; Kim, T.-W.; Wang, G. One-Dimensional Organic Artificial Multi-Synapses Enabling Electronic Textile Neural Network for Wearable Neuromorphic Applications. *Sci. Adv.* **2020**, *6* (28), No. eaba1178.
(58) Erb, R. J. Introduction to Backpropagation Neural Network Computation. *Pharm. Res.* **1993**, *10* (2), 165−170.
(59) Deng, L. The MNIST Database of Handwritten Digit Images for Machine Learning Research [Best of the Web]. *IEEE Signal Process. Mag.* **2012**, *29* (6), 141−142.
(60) Lecun, Y.; Bottou, L.; Bengio, Y.; Haffner, P. Gradient-Based Learning Applied to Document Recognition. *Proc. IEEE* **1998**, *86* (11), 2278−2324.
(61) Baum, E. B.; Wilczek, F. Supervised Learning of Probability Distributions by Neural Networks. In *Neural information processing systems*; Anderson, D. Z., Ed.; American Institue of Physics: denver, colorado, USA, 1987; pp 52−61.

https://doi.org/10.1021/acsnano.5c17016
ACS Nano 2026, 20, 1170−1180