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LETTER

Trapped charge modulation at the MoS_2/SiO_2 interface by a lateral electric field in MoS_2 field-effect transistors

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Abstract

Controlling trapped charges at the interface between a two-dimensional (2D) material and SiO_2 is crucial for the stable electrical characteristics in field-effect transistors (FETs). Typically, gate-source bias has been used to modulate the charge trapping process with a narrow dielectric layer with a high gate electric field. Here, we observed that charge trapping can also be affected by the lateral drain-source voltage (V_{DS}) in the FET structure, as well as by the gate-source bias. Through multiple V_{DS} sweeps with increasing measurement ranges of the V_{DS}, we demonstrated that the charge trapping process could be modulated by the range of the applied lateral electric field. Moreover, we inserted a hexagonal boron nitride (h-BN) layer between the MoS_2 and SiO_2 layer to explore the charge trapping behavior when a better interface is formed. This study provides a deeper understanding of controlling the electrical characteristics with interface-trapped carriers and lateral electrical fields in 2D material-based transistors.

1. Introduction

Atomically thin two-dimensional (2D) materials such as MoS_2, $MoSe_2$, WS_2, and WSe_2 have attracted tremendous attention as innovative nanoelectronic materials [1–4]. Among the 2D materials, MoS_2 is an excellent channel material for realizing 2D-based field-effect transistors (FETs) due to its outstanding electrical characteristics [5, 6] and intrinsic band gap feature (~1.9 eV for monolayer and 1.2 eV for bulk MoS_2) [7, 8]. In addition to these advantages, the MoS_2 FET shows good electrical stabilities from thermal [9, 10] and mechanical [11, 12] alterations, which are essential requirements for FETs. In spite of the innate stabilities of MoS_2, unstable electrical characteristics could be observed, caused by extrinsic sources. For example, trapped charges existing at the interface between MoS_2 and a gate dielectric layer (such as SiO_2) have been considered one of the dominant sources incurring electrically unsteady states [13, 14]. Occasionally, deliberate charge trapping at the interface between MoS_2 and SiO_2 or charge injection into SiO_2 has been used for materializing 2D material-based memory devices [15, 16]. Typically, to control trapping or detrapping electrons, gate-source bias has been used with a thin gate dielectric layer where a high gate electric field can be built [15, 16]. In our study, we observed that the charge trapping process in MoS_2 FETs could also be controlled by the measurement range of the lateral drain-source voltage (V_{DS}). Understanding altering electrical characteristics by the V_{DS} sweep range is considerably important for the realization of the stable electrical performance of FETs.

In addition to their advantages, trapped charges can function as Coulomb scattering sites and provide an effective gate-source bias, which can lead to fluctuating conductance [13, 14]. Therefore, large hysteresis in MoS_2 FETs induced by trapped charges can be an obstacle to practical applications in electronic devices. To avoid such obstacles, inserting a hexagonal boron nitride (h-BN) layer between MoS_2 and SiO_2 has been proposed to

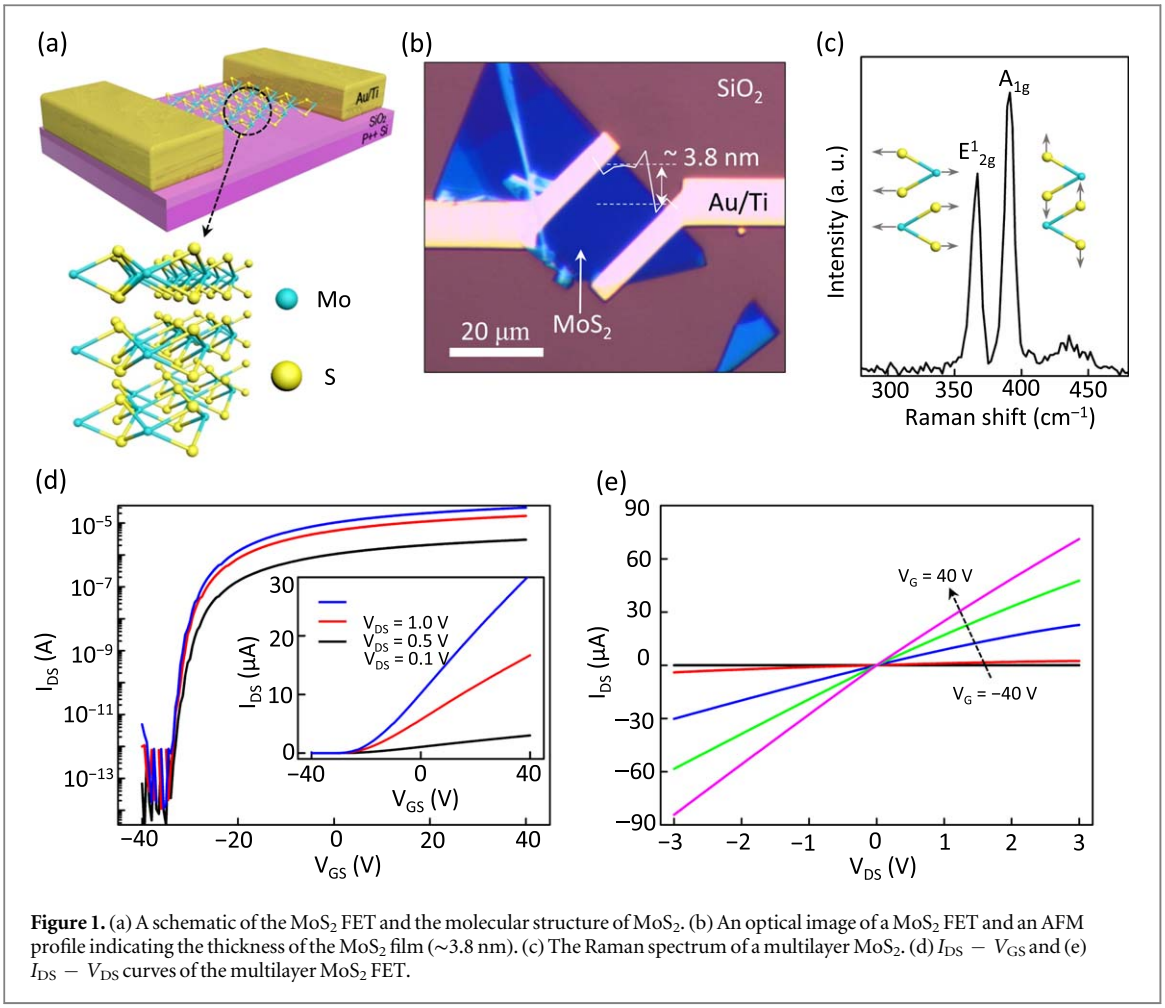

Figure 1. (a) A schematic of the MoS_2 FET and the molecular structure of MoS_2. (b) An optical image of a MoS_2 FET and an AFM profile indicating the thickness of the MoS_2 film (~3.8 nm). (c) The Raman spectrum of a multilayer MoS_2. (d) $I_{DS} - V_{GS}$ and (e) $I_{DS} - V_{DS}$ curves of the multilayer MoS_2 FET.

improve the interface condition due to its atomically flat surface without dangling bonds [17, 18]. Then, high carrier mobility was successfully achieved in 2D material-based FETs with such an h-BN buffer layer [17, 18].

Here, charge trapping and detrapping processes at the interface between MoS_2 and SiO_2 layers in MoS_2 FETs were investigated through multiple V_{DS} sweeps with increasing measurement ranges of the V_{DS}. We observed that electrons became trapped at the MoS_2/SiO_2 interface in the V_{DS} measurement range of up to 105 V, and then trapped electrons started to be withdrawn by a lateral electric field of ~67.3 kV cm^{-1}. Moreover, we fabricated a MoS_2 FET by inserting an h-BN buffer layer between the MoS_2 and SiO_2 layers and compared the electrical characteristics of these MoS_2 FETs with those of MoS_2 FETs without an h-BN layer. The carrier mobility of the MoS_2 FET with the h-BN layer showed a higher value (~52.7 $cm^2 V^{-1} \cdot s^{-1}$) than those of all the MoS_2 FETs without the h-BN layer characterized in this work (ranging from 0.5 $cm^2 V^{-1} \cdot s^{-1}$ to 46.0 $cm^2 V^{-1} \cdot s^{-1}$), and the hysteresis disappeared when a better interface was formed between the semiconductor and gate dielectric layer.

2. Results and discussion

Figure 1(a) shows a schematic of the multilayer MoS_2 FET device and the molecular structure of MoS_2. An optical image of a fabricated MoS_2 FET is shown in figure 1(b). The thickness of the mechanically exfoliated MoS_2 film (~3.8 nm) was measured by atomic force microscopy (AFM). The Raman peak positions of E^1_{2g} and A^1_g correspond to the in-plane and out-of-plane lattice vibrations, respectively, and the value of the frequency difference (~24 cm^{-1}) indicates an uncontaminated multilayer MoS_2 sheet (figure 1(c)) [19]. Detailed fabrication processes are explained in the supplementary information (figure S1 is available online at stacks.iop.org/NANOF/3/011002/mmedia) and experimental details section. Figures 1(d) and (e) exhibit the transfer curve (drain-source current versus gate-source voltage, I_{DS}–V_{GS}) and the output curve (drain-source current versus drain-source voltage, I_{DS}–V_{DS}) of a multilayer MoS_2 FET measured in vacuum (~10^{-4} Torr) at room temperature. These data showed good *n*-type semiconductor behavior with a high on/off ratio of over 10^9 and carrier mobility of 29.3 $cm^2 V^{-1} \cdot s^{-1}$. The carrier mobility as a function of V_{GS} is indicated in figure S2 in the supplementary information. Note that all the mobility values in this work

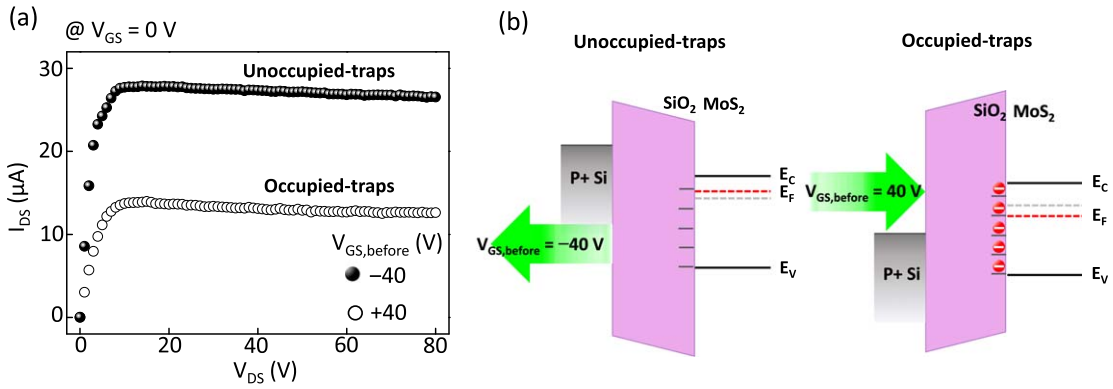

Figure 2. (a) $I_{DS} - V_{DS}$ curves of the multilayer MoS_2 FET illustrating two different electrical configurations (occupied-traps state and unoccupied-traps state) measured at $V_{GS} = 0$ V controlled by an initial gate-source voltage pulse ($V_{GS,before}$). (b) Schematic band diagrams illustrating the two different electrical configurations when $V_{GS,before} = -40$ or 40 V is applied.

signify the maximum values measured at V_{DS} in the linear region. The carrier mobility (μ) was calculated by the formula $\mu = (dI_{DS}/dV_{GS}) \times [L/(WC_iV_{DS})]$, where W (~25 μm) is the channel width, L (~15.6 μm) is the channel length, and $C_i = \varepsilon_o\varepsilon_r/d = 1.3 \times 10^{-4}$ F · m^{-2} is the capacitance between the MoS_2 and heavily doped Si back gate per unit area. Here, ε_o is the vacuum permittivity, ε_r (~3.9) is the dielectric constant of the SiO_2 dielectric, and d is the thickness (270 nm) of the SiO_2 layer.

To investigate the trapped charge effect on electrical characteristics, we applied a finite gate-source voltage pulse (denoted as $V_{GS,before}$) of −40 V or 40 V for one second before the actual measurement and then examined the output curve at a zero gate-source voltage ($V_{GS} = 0$). Figure 2(a) indicates that two different electrical configurations were observed: one with a higher saturation current (represented by filled circular symbols) and another with a lower saturation current (represented by open circular symbols), which are controlled by $V_{GS,before}$ (figure 2(a)). The origin of the two separate configurations can be explained by the effect of trapped electrons induced by $V_{GS,before}$. Because the MoS_2 channel and SiO_2 dielectric form an incomplete interface, trapped electrons could exist at the interface of MoS_2/SiO_2, which influences the channel current flow. This result is consistent with previous studies in which V_{GS} was used to control charge trapping by taking advantage of a narrow dielectric layer (a few hundred nanometers) with a high gate electric field [13, 14]. To classify two different configurations clearly, we applied the strong voltage of $V_{GS,before}$ (−40 V or 40 V). As shown in figure 2(b), when $V_{GS,before} = -40$ V was applied, the trapped electrons escaped from the trap sites at the interface to the MoS_2 channel. On the other hand, when $V_{GS,before} = 40$ V was applied, some free electrons were trapped at the trap sites at the interface. These two electrical configurations are denoted as the unoccupied-traps state and occupied-traps state, respectively (figures 2(a) and (b)). The trapped electrons induced by $V_{GS,before}$ caused Coulomb scattering with the free carriers (conduction electrons) in the MoS_2 channel and acted as a negative gate-source bias during the measurement, even at a fixed value of $V_{GS} = 0$ V, leading to reduced conductivity in the MoS_2 channel (figure 2(a)).

Similar to the above method using a gate-source voltage, trapped charges can also be controlled by a lateral electric field (i.e. a drain-source voltage). Figure 3(a) shows the output curves of a multilayer MoS_2 (12 nm-thick) FET under a series of V_{DS} sweeps with an increasing measurement range from 40 V (from 0 V to 40 V) to 130 V (from 0 V to 130 V) at a fixed $V_{GS} = 0$ V. Each V_{DS} sweep with increasing measurement ranges was performed in sequence without interval time. We fixed $V_{GS} = 0$ V, so that the channel current does not flow too much in the MoS_2 channel, even at high V_{DS} range, which avoids a permanent breakdown phenomenon by the Joule heating effect. When the measurement range increased from 40 V (from 0 V to 40 V, black filled circular symbols) to 105 V (from 0 V to 105 V, violet filled circular symbols), the saturation current gradually decreased from ~130 nA to ~30 nA, as shown in figures 3(a) and (b). In contrast, the saturation current continuously increased in V_{DS} sweeps from the measurement range of above 110 V (from 0 V to 110 V, gray open circular symbols). The decreased saturation current during the V_{DS} sweeps up to the measurement range of 105 V is ascribed to the charge trapping process because the free electrons can be trapped in the trap sites at the MoS_2/SiO_2 interface, and so the trapped electrons negatively affect the saturation current on the next V_{DS} sweep measurement (represented by the trapping process shown in figure 3(b)). After the V_{DS} sweep of 105 V (violet filled circular symbols), the trapped electrons started to be detrapped out of the trap sites owing to the strong lateral drain-source electric fields, which resulted in an increased saturation current in the next V_{DS} sweep measurement ranges from 110 V to 130 V (represented by the detrapping process shown in figure 3(b)). To calculate the energy levels of trap sites, we utilized the simplified Poole–Frenkel model in which the trapped charge can begin to

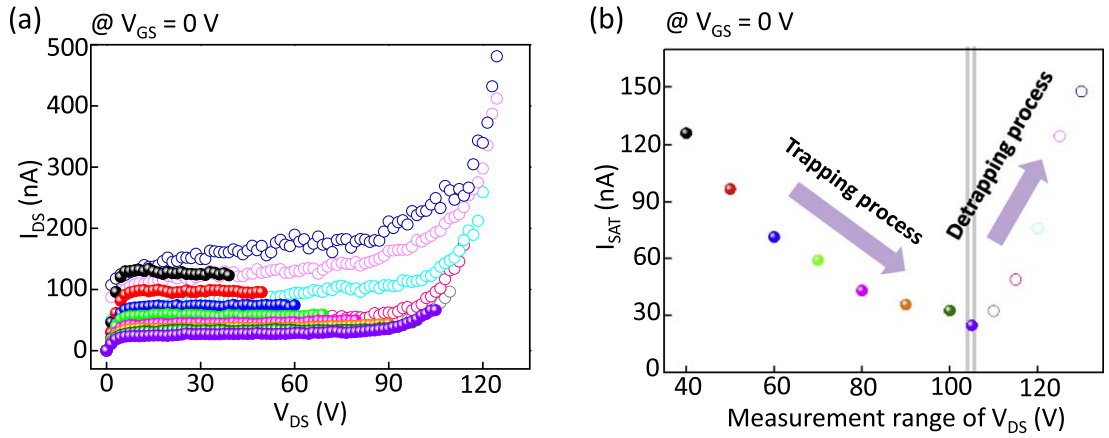

Figure 3. (a) $I_{DS} - V_{DS}$ curves under multiple V_{DS} sweeps with increasing measurement V_{DS} ranges from 40 V (from 0 V to 40 V) to 130 V (from 0 V to 130 V) at $V_{GS} = 0$ V. (b) Saturation current as a function of the measurement V_{DS} range at $V_{GS} = 0$ V. Black, red, blue, green, magenta, orange, dark green, and violet filled circular symbols correspond to the V_{DS} sweep ranges of 40, 50, 60, 70, 80, 90, 100, and 105 V, respectively, for the trapping process. Gray, pink, cyan, light pink, and navy open circular symbols correspond to the V_{DS} sweep ranges of 110, 115, 120, 125, and 130 V, respectively, for the detrapping process.

escape the potential barrier via thermionic-field emission at $V_{DS} = 105$ V. From the calculation, it was determined that the trapped electrons in trap sites would be located more than 72 meV away from the conduction band, which is in accordance with a previous study [20] (see figure S3 for details in the supplementary information). The schematics for describing the trapping and detrapping processes by multiple V_{DS} sweeps with different measurement V_{DS} ranges are illustrated in the supplementary information (figure S4). Note that the abrupt increase in the channel current above 110 V is due to the avalanche breakdown process under strong lateral electric fields [21].

To clearly identify whether the origin of the change in saturation current in response to the different V_{DS} sweep ranges was due to trapped charges, we further investigated and compared the saturation currents obtained from the repeated measurements under the occupied-traps state or unoccupied-traps state. Before the actual measurement, the occupied-traps or unoccupied-traps states were formed by applying $V_{GS,before} = 40$ V or -40 V, respectively (figures 4(a) and (b)). In the occupied-traps state (after applying $V_{GS,before} = 40$ V), the saturation current gradually increased and became saturated during the multiple V_{DS} sweeps from 0 V to 105 V at a fixed value of $V_{GS} = 0$ V, as shown in figure 4(a). This phenomenon is attributed to the detrapping process by the high lateral drain-source electric field (~67.3 kV cm^{-1}). Note that quite a high V_{DS} over 105 V was required for the detrapping process due to the long channel length (~15.6 μm) of our FET, and the range of the V_{DS} depends on the channel length of each device. The electrons escaped from the trap sites by the multiple V_{DS} sweeps, which gradually changed from the occupied-traps state to the unoccupied-traps state. The schematics of the detrapping processes by the multiple V_{DS} sweeps, explaining the results of figure 4(a), are illustrated in the supplementary information (figure S5). On the other hand, in the unoccupied-traps state (after applying $V_{GS,before} = -40$ V), the saturation currents did not change during the multiple V_{DS} sweeps because of a lack of electrons in the trap sites at the interface, as shown in figure 4(b). Figure 4(c) summarizes the values of the saturation currents during multiple V_{DS} sweeps in the occupied-traps and unoccupied-traps states. The difference in saturation current after the six repeated measurements between the occupied-traps state (~38 nA) and unoccupied-traps state (~67 nA) signifies the influence of the trapped electrons remaining after repeated measurements.

As mentioned in the introduction, understanding the control of trapped electrons is required for the stable electrical characteristics of MoS_2-based transistors or memory devices. In particular, a better interface between MoS_2 and the dielectric layer should be formed to avoid fluctuating conductance by trapped charges. In this manner, we inserted the h-BN layer between MoS_2 and SiO_2 to form an ideal interface without dangling bonds. Figures 5(a) and (b) show the schematics of the multilayer MoS_2 FETs without and with h-BN between the MoS_2 and SiO_2 layers. The thicknesses of the multilayer MoS_2 for the data of figures 5(a) and (b) were found to be ~12 nm and ~18 nm, respectively. We could not use the same MoS_2 thickness to compare the charge trapping behavior in figure 5. Note that the electrical characteristics can be dependent on the MoS_2 thickness [22, 23], but the influence of charge trapping by the difference in the MoS_2 thickness has been reported to be unclear and disputable [24–27]. Therefore, a further study exploring charge trapping behavior with diverse MoS_2 thicknesses is needed to investigate the accurate thickness-dependency of charge trapping. The thickness of the h-BN layer for the data shown in figure 5(b) was ~19 nm. The optical images and Raman spectrum for the fabricated MoS_2 FET with the h-BN layer are shown in the supplementary information (figure S6). Figures 5(c) and (d) indicate

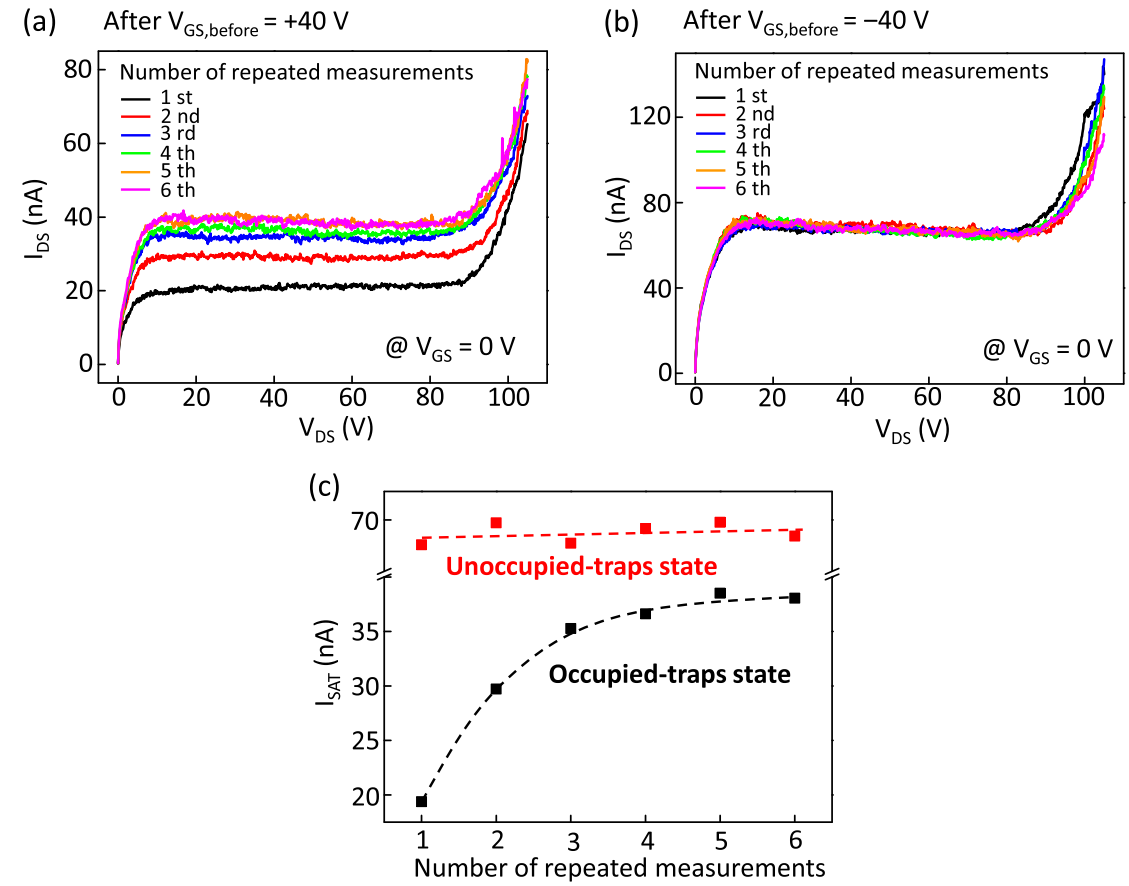

Figure 4. $I_{DS} - V_{DS}$ curves of the MoS_2 FET under repeated V_{DS} sweeps at $V_{GS} = 0$ V after (a) $V_{GS,before} = 40$ V or (b) $V_{GS,before} = -40$. (c) Saturation current versus number of repeated measurements for the two different electrical configurations (occupied-traps state and unoccupied-traps state).

the transfer curves of the MoS_2 FET without and with the h-BN layer measured in vacuum ($\sim 10^{-4}$ Torr) at room temperature. The mobility for the MoS_2 FET without the h-BN layer (figure 5(a)) and with the h-BN layer (figure 5(b)) was determined to be ~46.0 $cm^2 V^{-1} \cdot s^{-1}$ and 52.7 $cm^2 V^{-1} \cdot s^{-1}$, respectively. Here, a dielectric constant of 3.5 was used for the h-BN layer for the estimation of mobility values [4]. Note that the mobility of the MoS_2 FET with the h-BN layer showed a higher value than those of all the MoS_2 FETs without the h-BN layer (ranging from 0.5 $cm^2 V^{-1} \cdot s^{-1}$ to 46.0 $cm^2 V^{-1} \cdot s^{-1}$) characterized in this work. More importantly, hysteresis was not observed in the MoS_2 FET with the h-BN layer in contrast with the MoS_2 FETs without the h-BN layer because the h-BN layer forms a nearly ideal interface without dangling bonds and trap sites, as shown in figure 5(d). Note that in the hysteresis comparison between the two devices, we did not apply the same V_{DS} (figures 5(c) and (d)), but the charge trapping process is dominantly affected by V_{GS} rather than V_{DS} in our device because the electric field by V_{GS} is much stronger than that by V_{DS}. Therefore, the electrical characteristics did not change in the MoS_2 FETs with the h-BN layer regardless of whether $V_{GS,before} = 40$ V or −40 V (figure 5(f)), whereas the electrical characteristics changed for $V_{GS,before} = 40$ V compared to that for $V_{GS,before} = -40$ V for the MoS_2 FETs without the h-BN layer (figure 5(e)). These phenomena can be explained in detail with the schematic diagrams in the supplementary information (figure S7). For these reasons, inserting the h-BN layer between SiO_2 and MoS_2 is desirable for realizing the stable electrical characteristics in MoS_2 FETs.

3. Conclusions

In summary, we studied the influence of a lateral electric field on the charge trapping and detrapping dynamics at the interface between the MoS_2 and SiO_2 layers. From the results of multiple V_{DS} sweeps with increasing measurement ranges of the V_{DS}, it was found that the saturation current initially decreased in the low V_{DS} sweep range and then started to increase with a larger V_{DS} sweep range over 110 V. We demonstrated that this phenomenon was due to the charge trapping and detrapping processes originating from the imperfect interface between the MoS_2 and SiO_2 dielectric. In addition, we inserted an h-BN buffer layer between MoS_2 and SiO_2 to investigate the charge trapping effect after forming a near-ideal interface. Consequently, the hysteresis caused by

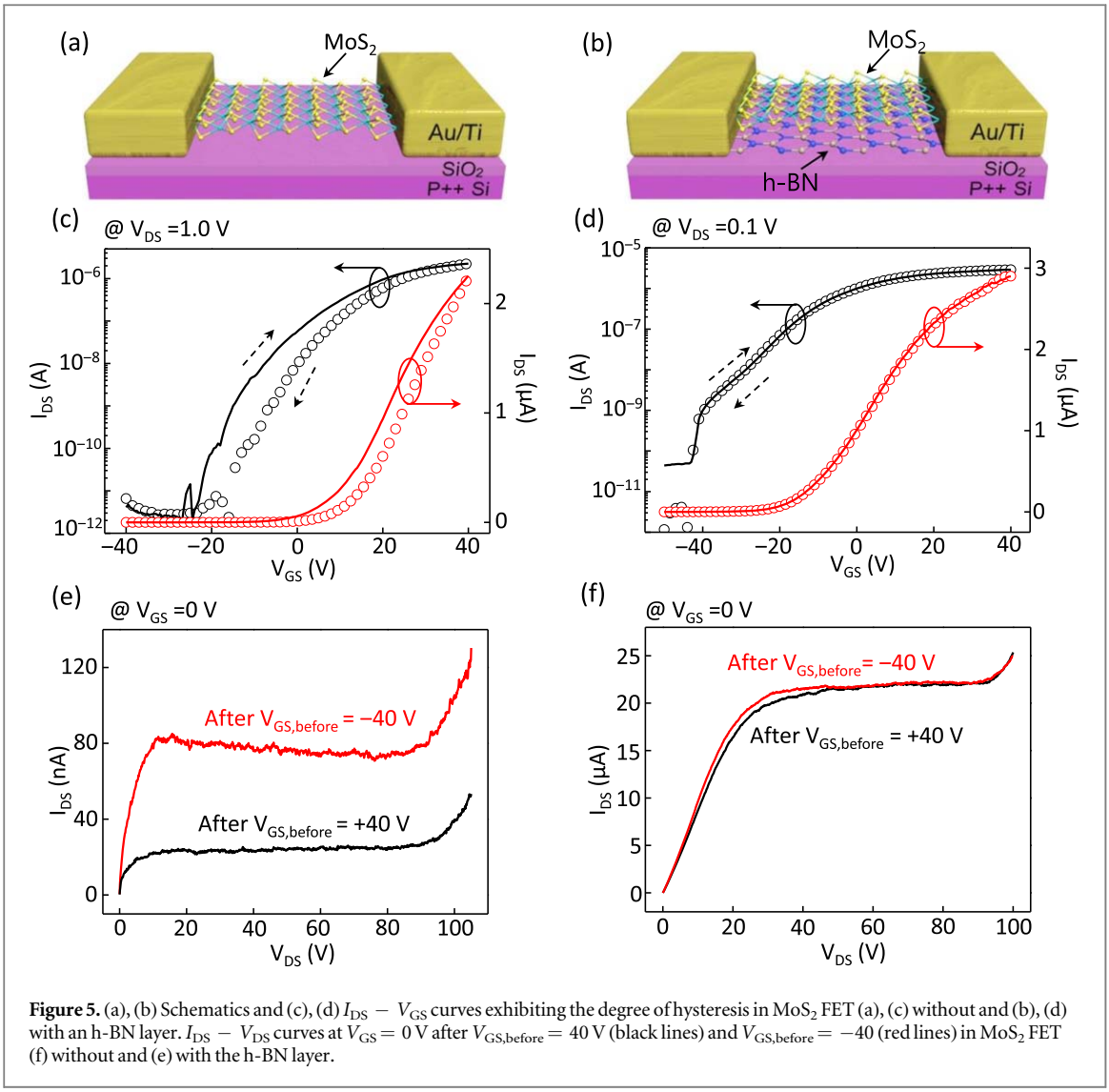

Figure 5. (a), (b) Schematics and (c), (d) $I_{DS} - V_{GS}$ curves exhibiting the degree of hysteresis in MoS_2 FET (a), (c) without and (b), (d) with an h-BN layer. $I_{DS} - V_{DS}$ curves at $V_{GS} = 0$ V after $V_{GS,before} = 40$ V (black lines) and $V_{GS,before} = -40$ (red lines) in MoS_2 FET (f) without and (e) with the h-BN layer.

trapped charges at the interface disappeared, and the trapped charge effect on electrical characteristics by $V_{GS,before}$ was also eliminated. This study provides a better understanding of the effect of interface-trapped carriers and controlling electrical characteristics by the lateral electric field in 2D material-based transistors.

4. Experimental details

4.1. Fabrication of MoS_2 FETs without and with an h-BN layer

MoS_2 films were transferred from a bulk MoS_2 crystal on a 270 nm-thick SiO_2/Si substrate by a mechanical exfoliation method. The electron resistor layer (poly(methyl-methacrylate) (PMMA) 950 K 11% concentration in anisole) was spin-coated at 4000 rpm and then it was annealed at 180 °C for 90 s on a hot plate for the preparation of electron beam lithography. An electron beam lithography system (JSM-6510, JEOL) was used for the drain and source patterns. Ti (5 nm) and Au (30 nm) were deposited using an electron beam evaporator (KVE-2004L, Korea Vacuum Tech.) sequentially.

To fabricate the MoS_2 FET with the h-BN layer, a micro-manipulator system (AP-4200GP, UNITEK) was used for transferring MoS_2 film on the h-BN layer. After transferring MoS_2 film on the h-BN layer, it was annealed at 120 °C for 30 m on a hot plate to remove water and oxygen molecules at the interface between MoS_2 and the h-BN layer. Next, an electron beam lithography system and an electron beam evaporator system were used for the formation of the source and drain electrodes as above.

4.2. Electrical characterization

The electrical properties of the MoS_2 FETs were measured using a semiconductor parameter analyzer (Keithley 4200-SCS) at various temperatures. Raman spectra of MoS_2 were characterized using an XperRam 200 (Nanobase, Inc.) instrument with a 532 nm laser as the excitation source.

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